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**Suresh et al.**

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(54) **OPTIMIZED SHA-256 DATAPATH FOR ENERGY-EFFICIENT HIGH-PERFORMANCE BITCOIN MINING**

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(51) **Int. Cl.**

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| ***H04L 9/06*** | (2006.01) |
| ***G09C 1/00*** | (2006.01) |

(52) **U.S. Cl.**

CPC ..... ***H04L 9/0643*** (2013.01); ***G09C 1/00*** (2013.01); *H04L 2209/12* (2013.01)

(58) **Field of Classification Search**

CPC ..... H04L 9/0643; H04L 2209/12; G09C 1/00
USPC ..... 713/181
See application file for complete search history.

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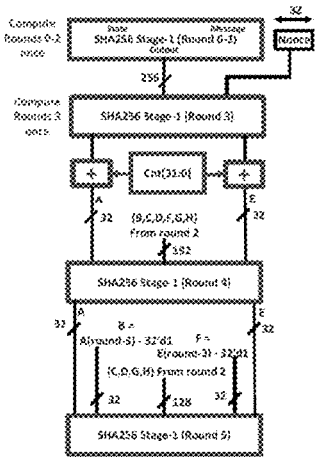
(57) **ABSTRACT**

A processing system includes a processor to construct an input message comprising a plurality of padding bits and a hardware accelerator, communicatively coupled to the processor, comprising a first plurality of circuits to perform a stage-1 secure hash algorithm (SHA) hash based on the input message, wherein the hardware accelerator comprises a first data path coupled between a first reference node and a first input node of the first plurality of circuits to feed a first padding bit of the plurality of padding bits to the first input node.

**16 Claims, 14 Drawing Sheets**