the base transceiver site **110** knows the transmitted RICH symbols and may then coherently sum the received symbols. Examples of non-coherent and coherent accumulation, which provide an estimate of the RICH symbol energy ($E_{s,rich}/I_o$), have been previously provided. In one embodiment, the SNR ($E_{s,rich}/N_t$) of the rate indicator channel R-RICH **426** may then be derived by taking the product of the RICH symbol energy ($E_{s,rich}/I_o$) and the inverse of the noise power spectral density (N_t/I_o), the equations of which have been also previously provided.

At block **840**, the processor **320** of the base transceiver site **110** determines the pilot SNR ($E_{c,pilot}/N_t$) of the pilot channel DPCCH **422** by taking the product of the measured SNR of the rate indicator channel R-RICH **426** and the inverse of the RICH-to-pilot ratio **730** for a particular data rate **710** over the traffic channel R-DPDCH **424** from the table **700** stored within memory **325** of the base transceiver site **110** as shown by the equation below.

$$\frac{E_{c,pilot}}{N_t} = \frac{E_{s,rich}}{N_t} \cdot \frac{E_{c,pilot}}{E_{c,rich}}$$

Once the SNR of the pilot channel DPCCH **422** is obtained, the pilot SNR may be used to perform inner-loop power control by the base transceiver site **110** for communicating with the mobile terminal **105** using methods well-established in the art.

At block **850**, the processor **320** of the base transceiver site **110** determines the symbol SNR ($E_{s,data}/N_t$) of the traffic channel R-DPDCH **424** by taking the product of the measured SNR of the rate indicator channel R-RICH **426**, the inverse of the RICH-to-pilot ratio **730**, and the traffic-to-pilot ratio **720** for a particular data rate over the traffic channel R-DPDCH **424** as shown by the equation below.

$$\frac{E_{s,data}}{N_t} = \frac{E_{s,rich}}{N_t} \cdot \frac{E_{c,data}}{E_{c,pilot}} \cdot \frac{E_{c,pilot}}{E_{c,rich}}$$

As previously mentioned, the RICH-to-pilot ratio **730** and traffic-to-pilot ratio **720** for a particular data rate **710** on the traffic channel R-DPDCH **424** are obtained from the table **700** stored within the memory **325** of the base transceiver site **110**. The estimated symbol SNR may then be used by the base transceiver site **110** for metric scaling in turbo decoding using methods well established in the art.

By keeping the signal power level of the pilot channel DPCCH **422** to a nominal signal power level to accommodate higher data rates over the traffic channel R-DPDCH **424** may cause the estimation of the SNR of the pilot channel DPCCH **422** to not be as precise as if it were transmitted at a higher signal power level. By measuring the SNR of the rate indicator channel R-RICH **426**, which is transmitted at a higher signal power level than the pilot channel R-DPCCH **422**, a more accurate estimation of the pilot channel SNR may be determined using the methods described above. As a result of achieving a more accurate SNR of the pilot channel DPCCH **422**, the wireless communication system **100** may achieve a more efficient inner-loop power control and symbol scaling for turbo decoding.

Those of skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

Those of skill would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

What is claimed is:

1. A method for a wireless communication system, comprising:

receiving a first signal over a first channel by a receiver and a second signal over a second channel by the receiver, said second signal received at a different signal power level than said first signal; and