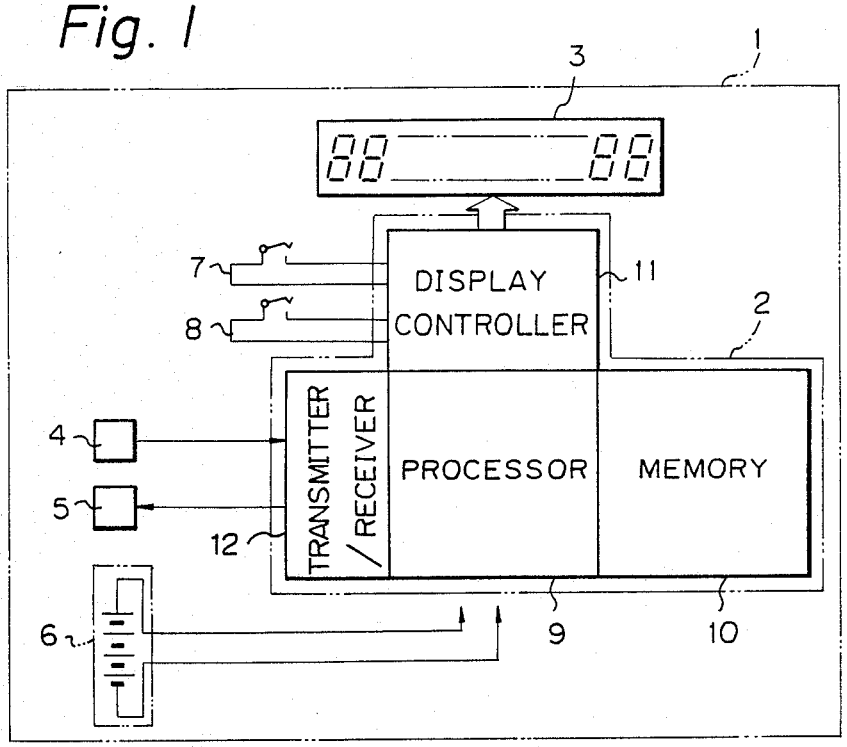
Fig. 1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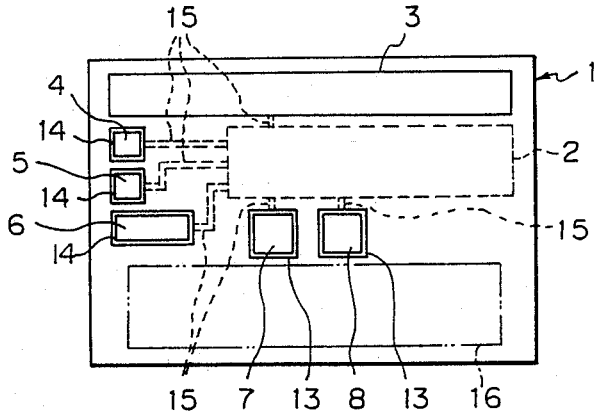
DISPLAY CONTROLLER
TRANSMITTER / RECEIVER
PROCESSOR
MEMORY

Fig. 2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