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Sorani et al.

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(54) **HARDWARE MICRO-SERVICES PLATFORM**

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G06F 9/445 (2018.01)
G06F 8/61 (2018.01)

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CPC ***G06F 9/44505*** (2013.01); ***G06F 8/61*** (2013.01)

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CPC G06F 9/44505; G06F 8/61; G06F 8/63; G06F 8/65; H03K 19/17756; H03K 19/17724; H03K 19/17736; H03K 19/17748; H03K 19/17752
See application file for complete search history.

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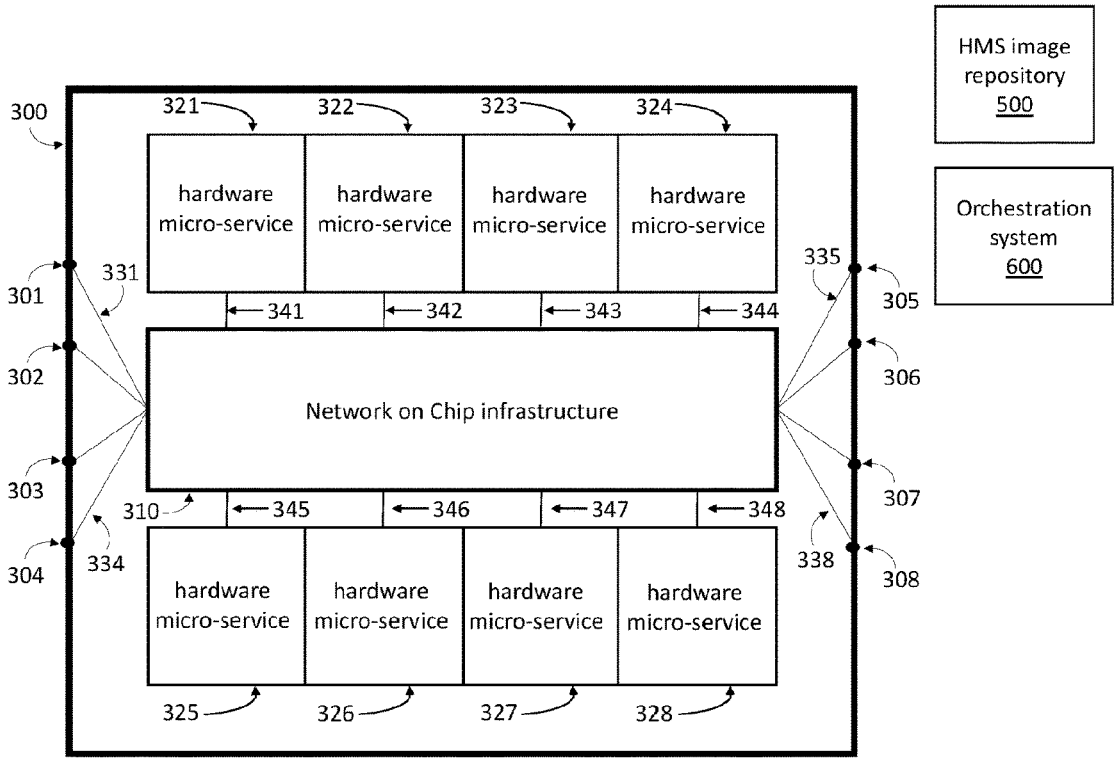
(57) **ABSTRACT**

A device comprising: at least one partially reconfigurable FPGA; a Network-on-Chip (NoC) comprised in the FPGA; and at least one area on the at least one FPGA operable to house a hardware micro-service (HMS); wherein an HMS image may be loaded onto the area of the at least one FPGA via partial reconfiguration to form a new HMS, and the NoC is operable to forward information to and from the new HMS without the NoC being reloaded.

17 Claims, 7 Drawing Sheets