chip phases of the B dominant long codes and stores them. In addition, since the information about the long code types to be searched has been provided in advance to a long code replica generator **25**A by the base station over the current control channel, the correlation detection and synchronization decision are made for B spreading codes. Thus, received signal levels are detected for the correlation outputs associated with B contiguous cells, followed by specifying the base station to which the channel is to be switched next.

FIG. **17** is a block diagram of a system corresponding to claims **5**, **6** and **7**, which operates as follows:

(With regard to claim **5**)

1. A long code synchronized phase detector **35** detects the long code synchronized phase as the blocks **21**–**24** in FIG. **7**. The reference numeral **80** designate a matched filter, **81** designates a short code replica generator, **82** designates a memory for correlation values and their timings, **83** designates a maximum correlation value selector (comparator) and **84** designates a memory.

2. The phase of a long code replica generator **36** is set at the synchronized phase detected by the circuit **35**.

3. An integrating/dumping circuit **37** integrates the correlation between the received spread modulation signal and a code obtained by multiplying the long code fed from the long code replica generator **36** by the short code fed from the short code replica generator **81**, and its output is square-law detected by a square-law detector **38**. The resultant correlation value and its corresponding long code type fed from the long code replica generator **36** are stored in the memory **39**.

4. The operation of the foregoing items **2** and **3** are repeated by changing the type of the long code fed from the long code replica generator **36**.

5. After detecting correlation for the entire long codes, a maximum correlation value selector **40** decides the long code giving the maximum correlation value as the long code for spreading the received signal, thus completing the acquisition.

(With regard to claim **6**)

In addition to the operation associated with claim **5**, the synchronization detection is completed if a comparator **41** makes a decision that the maximum value exceeds a threshold value, otherwise the acquisition is continued.

(With regard to claim **7**)

1. A threshold value determiner **42** is added for deciding the threshold value of claim **6** in response to the maximum correlation value detected by the long code synchronized phase detector **35**.

FIG. **18** is a block diagram corresponding to claim **8**, and operate s as follows:

1. As initial detection, a contiguous cell search circuit **43** as shown in FIG. **8** detects the synchronized long code phase and its long code type for each of B contiguous cells.

2. The synchronized long code phases and the long code types of the B contiguous cells are initially set in a long code replica generator **45** in a multipath detector **44**.

3. The received signal except for that of the first step is input to the multipath detector **44** by transferring a switch SW.

4. Multipath search is carried out by detecting correlation around the synchronized long code phase using a long code replica matched to each contiguous cell.

5. The multipath decision is made by integrating by integrating/dumping circuit **46** the correlation between the received spread modulation signal and a code obtained by multiplying the long code fed from the long code replica generator **45** by a short code fed from a short code replica generator **150**, by square-law detecting its output through a square-law detector **47**, and by making threshold decision of the power output from the square-law detector **47** by a threshold value decision circuit **48**.

6. A post-RAKE combining received power detector **49** makes a RAKE combining (path diversity) of the multipaths which exceed the threshold value, measures the received power and stores the measured power in a memory **50**.

7. A maximum multipath detector **51** detects the phase of the long code which gives the maximum power multipath of each cell.

8. After measuring the received power of all the contiguous cells, the cell giving the maximum post-RAKE combining received power is decided as the handover cell.

9. The output of the maximum multipath detector **51** is input to the long code replica generator **45** to update its long code phase to a newly synchronized long code phase which is equal to the long code phase of the maximum multipath among the contiguous cells.

10. Repeat the operation of item **3** and onward at fixed intervals.

FIGS. **19**A and **19**B are block diagrams corresponding to claim **22**, which operates as follows.

1. A selector **53** in a long code synchronized phase detector **52** detects not only a maximum correlation value but also its neighboring (within one symbol period, for example) correlation peaks.

2. A memory **84** stores phase differences (relative delays) between the long code synchronized phase obtained from the timing giving the maximum correlation value and the neighboring correlation peaks (paths).

3. The detected long code synchronized phase is set in a long code replica generator **55**, relative delays of the paths are set in delay circuits **56**, and the long code fed from the long code replica generator **55** is multiplied by the short code fed from a short code replica generator **81**.

4. Correlations, which are detected between the received spread modulation signal and the codes with relative delays provided by the delay circuits delaying the product of the long code and the short code, are integrated and square-law detected through integrating/dumping circuits **57** and square-law detectors **58**, and are added by an adder **59**.

5. A threshold value decision circuit **60** makes a threshold decision of the relative power obtained as the addition result, and decides whether the synchronization has been established or not. When not yet established, the operation of item **4** is repeated with changing the type of the long code.

6. (In claim **5**, the maximum value is selected after detecting the correlation power obtained as a result of the addition for each long code.)

FIG. **20** is a block diagram corresponding to claim **12**, which operates as follows.

1. At the initial acquisition stage, a long code synchronized phase detector **61** operates for detecting the long code synchronized phase.

2. A long code replica generator **62** is initially set at the detected long code synchronized phase so that the long code identification is carried out. The long code synchronized phase detection is continued as well.

3. The long code synchronized phase detector **61** includes a timer **63** so that the most recently detected long code synchronized phase is set in the long code replica generator **62**.

4. The same steps as those of other claims are taken for making correlation detection between the received spread modulation signal and the codes obtained by multiplying the long codes fed from the long code replica generator **62** and the short code fed from a short code replica generator **81**.