30. The method of claim **29**, further comprising translating the zero-offset-carrier frequency signal {s(n)} down to a baseband signal {w(n)}.

31. The method of claim **26**, wherein a sampling clock is derived from a VCXO that is phase-locked to a reference frequency.

32. The method of claim **26**, wherein a correlation is computed at lags which are commensurate with a sampling rate.

33. The method of claim **26**, wherein a matched filter is not employed.

34. The method of claim **26**, wherein the spectrum shaped channel pilot signal {γ(n)} is a spectrum shaped Q-channel pilot signal.

35. The method of claim **26**, wherein averaging includes averaging C_{MS} over multiple correlation computations to reduce noise.

36. The method of claim **26**, wherein correlations for lags smaller than the sampling interval are synthesized using digital signal processing.

37. The method of claim **36**, wherein using digital signal processing includes synthesizing an offset to improve precision of an estimate of time-of-arrival of a received pilot code.

38. The method of claim **26**, further comprising disciplining another oscillator in parallel to track multiple pilots including generating another spectrum shaped channel pilot signal by:

oversampling to yield another signal;

passing the another signal through another FIR filter; and

filtering with another second FIR filter to yield the another spectrum shaped channel pilot signal.

39. The method of claim **26**, further comprising time sharing a correlator circuit to track multiple pilots.

40. The method of claim **26**, wherein disciplining an oscillator includes generating another spectrum shaped channel pilot signal from another different chip-rate PN sequence.

41. An apparatus to track a pilot signal to discipline an oscillator, comprising:

a correlator circuit adapted to oversample a chip-rate PN sequence {i(n)} at a higher sampling rate to yield a signal {a(n)}, pass {a(n)} through a first FIR filter whose impulse response coefficients are {g(n)} to yield a signal {ϑ(n)}; and filter {ϑ(n)} with a second FIR filter to yield a spectrum shaped pilot channel signal {γ(n)}; and

a signal processor circuit coupled to the correlator circuit, wherein the signal processor circuit disciplines the oscillator and averages correlation values between the signal {a(n)} and the spectrum shaped channel pilot signal {γ(n)} over multiple periods of the chip-rate PN sequence to improve a quality of pilot position estimation.

42. The apparatus of claim **41**, wherein said correlator circuit includes a FPGA.

43. The apparatus of claim **41**, wherein said signal processor circuit includes a DSP.

44. The apparatus of claim **41**, further comprising an A/D converter coupled to said signal processor circuit.

45. The apparatus of claim **41**, wherein the first FIR filter includes a 4-point FIR filter having all 4 coefficients at least substantially equal.

46. The apparatus of claim **41**, wherein the second FIR filter includes a 48-point FIR filter.

47. The apparatus of claim **41**, further comprising an autonomous background correlator coupled to the correlator circuit.

48. A receiver comprising at least two of the apparatus according to claim **41** that are operated in parallel to track multiple pilots.

49. The apparatus of claim **16**, wherein the signal processor averages C_{MS} over multiple correlation computations to reduce noise.

50. The apparatus of claim **41**, wherein the signal processor averages C_{MS} over multiple correlation computations to reduce noise.

51. The apparatus of claim **41**, wherein the DSP synthesizes an offset to improve precision of an estimate of time-of-arrival of a received pilot code.

52. The apparatus of claim **41**, wherein the correlator circuit is time shared to track multiple pilots.

53. The apparatus of claim **41**, wherein the correlator circuit adapted to oversample another different chip-rate PN sequence.

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