United States Patent [19]

Myer et al.

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[54] **PARALLEL INTERCONNECT FOR PLANAR ARRAYS**

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[51] **Int. Cl.**[3] **H05K 1/08**

[52] **U.S. Cl.** ..... **339/17 N**; 339/49 B

[58] **Field of Search** ..... 339/17 CF, 17 M, 17 LM, 339/17 N, 18 R, 18 C, 48, 49 B, 252 R, 254 R, 254 M; 361/412

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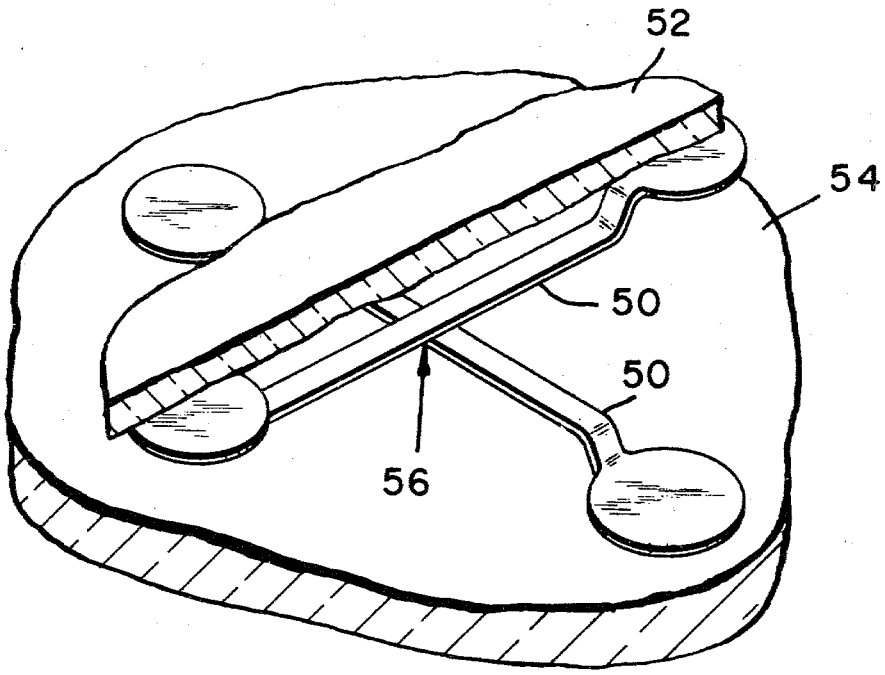
[57] **ABSTRACT**

A large scale parallel architecture in which many parallel channels numbering 10^2 or more operate simultaneously to create a natural and efficient organization for processing two-dimensional arrays of data. The architecture comprises a plurality of stacked integrated circuit wafers having top and bottom surfaces, electric signal paths extending through each of the wafers between the surfaces, and micro-interconnects (smaller than 50 mil) on the surfaces of adjacent wafers interconnecting the respective electric signal paths with a topographical one-to-one correspondence.

7 Claims, 14 Drawing Figures