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(12) **United States Patent**
Sherrer

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(54) **DEVICE PACKAGE AND METHODS FOR THE FABRICATION AND TESTING THEREOF**

G02B 6/4239; G02B 6/4248; G02B 6/4292;
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See application file for complete search history.

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(57) **ABSTRACT**

Provided are methods of forming sealed via structures. One method involves: (a) providing a semiconductor substrate having a first surface and a second surface opposite the first surface; (b) forming a layer on the first surface of the substrate; (c) etching a via hole through the substrate from the second surface to the layer, the via hole having a first perimeter at the first surface; (d) forming an aperture in the layer, wherein the aperture has a second perimeter within the first perimeter; and (e) providing a conductive structure for sealing the via structure. Also provided are sealed via structures, methods of detecting leakage in a sealed device package, sealed device packages, device packages having cooling structures, and methods of bonding a first component to a second component.

(52) **U.S. Cl.**

CPC **G01B 11/16** (2013.01); **G01B 11/26** (2013.01); **G02B 6/4201** (2013.01); **G02B 6/421** (2013.01); **G02B 6/423** (2013.01); **G02B 6/4204** (2013.01);

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7 Claims, 26 Drawing Sheets

(58) **Field of Classification Search**

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