# BACKSIDE SOURCE-DRAIN CONTACT FOR INTEGRATED CIRCUIT TRANSISTOR DEVICES AND METHOD OF MAKING SAME

## CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional application from U.S. Application for patent Ser. No. 14/298,000 filed Jun. 6, 2014, the disclosure of which is incorporated by reference.

## FIELD OF THE INVENTION

The present disclosure generally relates to integrated circuits and, in particular, to integrated circuits with transistors formed with a small pitch.

## BACKGROUND

Those skilled in the art understand that integrated circuit dimensions are becoming increasingly smaller. As the technology nodes for fabrication continue to scale down, it is becoming increasingly more difficult to prevent short channel effects (SCE) in the transistor and reduce the resistance of metal lines in order to reach required performance characteristics for device speed performance. Additionally, the reduced pitch of the transistor layout complicates the ability to make electrical contact to the source and drain regions from above the transistor.

It is known in the art to fabricate transistors on an integrated circuit substrate which is of the Silicon-on-Insulator (SOI) type (as opposed to the use of bulk semiconductor substrates). An SOI substrate is formed of a top semiconductor (for example, silicon or silicon-germanium) layer over an insulating (for example, silicon dioxide) layer over a bottom semiconductor (for example, silicon) substrate layer. The source, drain and channel of the transistor are formed in the top semiconductor layer. The resulting transistor is electrically insulated from the lower part of the substrate by the intermediate layer of insulating material. This structure advantageously reduces concerns with leakage current.

Further substrate development has reduced the thickness of the intervening insulating layer to about 50 nm to produce a substrate for use in transistor fabrication that is referred to as an extremely thin silicon on insulator (ETSOI) substrate. Still further substrate development has reduced the thicknesses of all substrate layers to produce a substrate for use in transistor fabrication that is referred to an ultra-thin body and buried oxide (UTBB) substrate where the thickness of the intervening insulating layer is about 25 nm (or less) and the thickness of the top semiconductor layer is about 5 nm to 10 nm. All of these substrates may more generally be referred to as SOI substrates.

Notwithstanding the recognized advantages of using SOI substrates for transistor fabrication, it is noted that some variation in layer thickness can occur, especially in the case of the ETSOI substrate and the UTBB substrate. This variation in layer thickness can lead to variability in both threshold voltage (Vt) roll-off and sub-threshold voltage slope for transistors fabricated on and in the substrate. This variability is especially a concern for transistors having gate lengths of less than about 25 nm.

There is accordingly a need in the art for an alternative means to make a transistor supported by a SOI-type substrate.



## SUMMARY

In an embodiment, an integrated circuit transistor comprises: a substrate including an insulating layer and an overlying semiconductor layer, the substrate including a trench extending into the insulating layer; a metal material at least partially filling the trench in the insulating layer to form a source contact buried in the substrate; a source region formed by the overlying semiconductor layer, said source region lying on top of and in electrical contact with the source contact; a channel region in the overlying semiconductor layer adjacent the source region; a gate dielectric on top of the channel region; and a gate electrode on top of the gate dielectric.

In an embodiment, a method comprising: forming a trench in a substrate; at least partially filing said trench with a metal material form a source contact buried in the substrate; epitaxially growing a source region over the source contact; epitaxially growing a channel region located adjacent the source region; providing a gate dielectric on top of the channel region; and forming a gate electrode on the gate dielectric.

In an embodiment, a method comprises: forming a trench extending into a substrate including an insulating layer and a semiconductor layer, wherein said trench extends through the semiconductor layer and at least partially into the insulating layer; partially filling the trench in the insulating layer with a metal material to form a source contact; epitaxially growing semiconductor material from said semiconductor layer to cover a top of the source contact with a source region; converting the semiconductor layer adjacent the source region to form a channel region; and forming an insulated gate electrode over the channel region.

In an embodiment, a method comprises: forming a trench in a substrate including an insulating layer and an overlying semiconductor layer, the substrate including a trench extending into the insulating layer; at least partially filling the trench in the insulating layer with a metal material to form a source contact; forming a source region made of semiconductor material adjacent the overlying semiconductor layer and lying on top of and in electrical contact with the source contact; forming a channel region from the overlying semiconductor layer adjacent the source region; forming an insulated gate electrode over the channel region.

The foregoing and other features and advantages of the present disclosure will become further apparent from the following detailed description of the embodiments, read in conjunction with the accompanying drawings. The detailed description and drawings are merely illustrative of the disclosure, rather than limiting the scope of the invention as defined by the appended claims and equivalents thereof.

## BRIEF DESCRIPTION OF DRAWINGS

Embodiments are illustrated by way of example in the accompanying figures not necessarily drawn to scale, in which like numbers indicate similar parts, and in which:

FIG. **1** is a cross-sectional diagram of a plurality of transistors which utilize a backside contact made to the transistor source-drain regions;

FIGS. **2**A-**2**Q illustrate process steps for forming the integrated circuit shown in FIG. **1**;

FIG. **3** is a cross-sectional diagram of a plurality of transistors which utilize a backside contact made to the transistor source-drain regions;

FIGS. **4**A-**4**B illustrate alternative process steps for forming the integrated circuit shown in FIG. **3**;