

1

SEMICONDUCTOR DIE PACKAGE WITH INCREASED THERMAL CONDUCTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is generally in the field of semiconductor die packaging.

2. Related Art

During semiconductor packaging, dice are mounted onto a die pad fabricated on a surface of a substrate. After a die is mounted on the substrate, bond wires are used to electrically connect die bond pads located on the die to their corresponding substrate ground pads and substrate signal pads located on the substrate. Vias in the substrate provide a connection between the substrate die pad and a heat spreader situated on a bottom surface of the substrate. This connection may also have an electrical function. Vias also provide a connection between substrate signal pads to corresponding substrate signal lands situated on the bottom surface of the substrate.

An important function carried out by the substrate is that of dissipating heat generated by the die during operation. A multilayer substrate is desirable because it allows increased circuit design flexibility; however, this can also increase the path required for thermal conduction, which decreases the heat dissipating ability of the package. In general, the substrate provides a thermal conduction path away from the die by way of the substrate die pad through vias connecting the substrate die pad to the heat spreader, and through the heat spreader to, for example, a printed circuit board ("PC board" or "PCB"). However, due to the arrangement of conventional substrates as well as the fabrication process associated with conventional substrates, the thermal conduction path through the semiconductor package is severely limited. By way of example, thermal conduction is particularly limited in multi-layer substrates, such as four-layer substrates. As a consequence of inefficient thermal conduction, heat dissipation is severely limited and, therefore, semiconductor devices using such packages can suffer from poor performance and poor package reliability. Moreover, this problem is exacerbated where Gallium Arsenide (GaAs) dice are used. GaAs die have a much lower thermal conductivity (45 W/mK) compared to Si (160 W/mK) and, as a result, the thermal conduction inefficiency of conventional packages presents even more of a problem for GaAs devices.

Accordingly, there is a strong need in the art for a packaging structure and method which provides increased thermal conduction. More particularly, there is a need in the art for a packaging structure and method which provides increased thermal conduction in a multi-layer substrate.

SUMMARY OF THE INVENTION

The present invention is directed to a semiconductor die package with increased thermal conduction. The invention overcomes the need in the art for a structure which provides increased thermal conduction in a semiconductor die package and, in particular, in a semiconductor die package with a multi-layer substrate.

In one exemplary embodiment, a structure comprises a multilayer substrate having a core, a top surface and a bottom surface. A substrate die pad is situated on the top surface of the substrate and is capable of receiving a die, and

2

a heat spreader is situated on the bottom surface of the substrate. The substrate die pad and the heat spreader may also perform electrical functions. The substrate further comprises at least one buried via within the core. The at least one buried via is situated below a first metal cap, and a second metal cap is situated below the at least one buried via. In one embodiment, the diameter of the at least one buried via is approximately 100–200 microns, and the length of the at least one buried via is approximately 100–200 microns. In one particular embodiment, the at least one buried via is plated with a metal barrel, where, for example, the thickness of the metal barrel is approximately 15–50 microns.

The first metal cap is thermally coupled to the substrate die pad, and the second metal cap is thermally coupled to the heat spreader. In one particular embodiment, the first and second metal caps comprise copper. With this arrangement, the at least one buried via provides a connection between the substrate die pad and the heat spreader which results in substantially increased thermal conduction between the substrate die pad and the heat spreader due to the shorter thermal conduction path through the at least one buried via while maintaining a multilayer structure on the remaining substrate area.

According to one exemplary embodiment, the substrate further comprises a first intermediate metal layer and a second intermediate layer. The first intermediate layer is situated between and thermally couples the first metal cap and the at least one buried via, and the second intermediate metal layer is situated between and thermally couples the at least one buried via and the second metal cap. The first intermediate metal layer and the first metal cap appear as and are indistinguishable in function from a single metal layer. Likewise, the second intermediate metal layer and the second metal cap appear as and are indistinguishable in function from another single metal layer.

According to one embodiment, the present invention is a method for fabricating the above described exemplary semiconductor die packaging structure. Other features and advantages of the present invention will become more readily apparent to those of ordinary skill in the art after reviewing the following detailed description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A illustrates a cross-sectional view of a known semiconductor die packaging structure.

FIG. 1B illustrates a top view of an exemplary via in the structure of FIG. 1A.

FIG. 2 illustrates a flowchart of an exemplary process by which an embodiment of the present invention is fabricated.

FIG. 3A illustrates a cross-sectional view, which includes portions of an exemplary structure fabricated according to an embodiment of the invention and a corresponding process step of the flowchart of FIG. 2.

FIG. 3B illustrates a cross-sectional view, which includes portions of an exemplary structure fabricated according to an embodiment of the invention and a corresponding process step of the flowchart of FIG. 2.

FIG. 3C illustrates a cross-sectional view, which includes portions of an exemplary structure fabricated according to an embodiment of the invention and a corresponding process step of the flowchart of FIG. 2.

FIG. 3D illustrates a cross-sectional view, which includes portions of an exemplary structure fabricated according to an embodiment of the invention and a corresponding process step of the flowchart of FIG. 2.