APPARATUS AND METHOD TO COMPENSATE FOR UNSYNCHRONIZED TRANSMISSION OF SYNCHROUS DATA USING A SORTED LIST

TECHNICAL FIELD

This invention relates to the transmission of digitally encoded voice, and in particular, to the transmission of digitally encoded voice between a circuit switching network and a packet switching network so as to maintain speech quality.

BACKGROUND OF THE INVENTION

In the transmission of digitally encoded voice, it is important to maintain synchronization between the two end points so that no digital information is lost due to differing rates of transmission and reception. Synchronization is the ability to maintain a stable frequency and precise timing to allow digital transmission services to read data out and read data into the transmission system at the same rate. Without synchronization, rates differ and data slippage occurs resulting in data being lost. Within the prior art, circuit switch networks and packet data switching networks when operating independently of each other have solved this problem in the following manner. In circuit switched networks, synchronization is centrally located and is synchronized throughout continental United States. For example, long distance transmission carriers, such as AT&T, have placed synchronization technologies in there central offices and relied on T1 trunk-based recovery network timing subsystems to synchronize data being received from the network. Packet switched network have allowed the receiving endpoint to signal the transmitting endpoint to slow or speed-up the transmission rate. This type of control is utilized in asynchronous transfer mode (ATM) and frame relay transmission (FR). However, the internet protocol (IP) transmission systems provide no such synchronization mechanism even though they are packet switched networks.

The prior art methods for achieving synchronization in circuit switched networks and packet switched network performed well if the two types of networks were not interconnected. An exception to this situation was in the situation where ATM or frame relay was utilized with a circuit switched network with the same data transmission company controlling both systems. Within the present business communication switching environment, there exists a need for simplified maintenance, management, and access to voice information on diverse networks. This need is forcing the convergence of a variety of circuit switched and packet switched networks. In addition, a new class of real-time multimedia networks is emerging that will also require synchronization.

The combination of a circuit switched network and a packet switched network is referred to as a hybrid network. Hybrid networks that lack synchronization exhibit the same symptoms as if packets were being lost within a packet switching system with some asymmetry. (1) If the read-out is faster than the read-in, eventually the reader exhausts the jitter-buffers and must wait for them to refill. The voice coder sees an empty stream of voice information and hence the voice quality suffers remarkably. (2) If the read-out is slower than the read-in, eventually the jitter-buffers fill full, and new packets are discarded. The voice coder sees a loss of packets and again the voice quality suffers.

A prior art solution for interconnecting a hybrid network is illustrated in FIG. **1**. Synchronous physical (PHY) interface **101** is reading out PCM voice samples to voice coder **106** via path **114**. Voice coder **106** transmits these PCM

packets via path **113** to IP switched network **107**. IP switch network **107** transmits packets containing PCM samples to voice coder **106** which transmits these to PHY **101** via elements **102**, **103**, and **104** and paths **108**, **109**, and **111**. PHY **101** utilizes insert/remove circuit **102** to obtain the packets that are being placed in sampled queue **104** by voice coder **106**. Insert/remove circuit **102** adds or deletes PCM samples as required to maintain a synchronous transfer of data to PHY **101**. Insert/remove circuit **102** performs this activity by utilizing low energy detector **103**. Low energy detector **103** evaluates the PCM sample that will next be transmitted from sample queue **104** to circuit **102** via path **109**. Low energy detector **103** indicates to circuit **102** if the energy contained within the PCM sample is below a predefined threshold and may be discarded. If there is not a sample present in sample queue **104** and a sample is required to be transmitted to PHY **101**, insert/remove circuit **102** transmits a low energy PCM sample. When insert/remove circuit **102** has to delete samples being received from sample queue **104**, circuit **102** deletes any present sample indicated by low energy detector **103** as being below predefined energy value requirement. Circuit **102** commences this operation at some predefined capacity of sample queue **104**. The problem with this prior art solution is that insert/remove circuit **102** has no knowledge of the number or location of PCM samples that are below the predefined energy value within sample queue **104**. Hence, for example, if circuit **102** determines that it must delete five PCM samples, circuit **102** will delete the next five PCM samples that low energy detector **103** indicates are below the minimum energy level. This can result in deletion of samples over a small period of time and cause deterioration of the voice quality being produced by PHY **101**.

SUMMARY OF THE INVENTION

This invention is directed to solving these and other problems and disadvantages of the prior art. In an embodiment of the invention, the low energy detector maintains a sorted list that defines to the circuit removing samples from the queue the location and energy of all samples that fall below the predetermined energy level. This allows the circuit removing samples to execute an algorithm that allows samples to be deleted in accordance with a predetermined pattern.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** illustrates a prior art system;

FIG. **2** illustrates a first embodiment of the invention;

FIG. **3** illustrates a second embodiment of the invention;

FIG. **4** illustrates, in block diagram form, insert/removal circuit of FIG. **3**;

FIG. **5** illustrates, in block diagram form, low energy detector and low energy detector;

FIGS. **6**, **7** and **8** illustrate, in flowchart form, the steps performed by insert/removal circuit in implementing the first embodiment of the invention;

FIG. **9** illustrates, in flowchart form, the steps performed by low energy detector in implementing the first embodiment of the invention;

FIG. **10** illustrates a sort list table used in implementing the second embodiment of the invention;

FIGS. **11** and **12** illustrate, in flowchart form, the operations performed by insert/removal circuit in implementing the second embodiment of the invention;

FIG. **13** illustrates, in flowchart form, the operations performed by a low energy detector in implementing the second embodiment of the invention; and