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NON-DISRUPTIVE SELECTIVE TRAFFIC BLOCKING IN A SAS DOMAIN

TECHNICAL FIELD

The present invention relates to serial attached SCSI (SAS) domains and, more particularly, to a SAS expander with configurable register bits to selectively block traffic from physical I/O devices.

BACKGROUND

In a SAS domain, discovery I/O operations must compete with all other I/O operations. A problem can arise when the I/O traffic level is so high that it crowds out the discovery traffic, which can in turn make it difficult for discovery to complete in a timely manner. In some cases, discovery may not complete at all as a result of the congestion. Even in the best case, discovery in large topologies can take more time than is desired. There is, therefore, a continuing need for selectively blocking I/O traffic in a SAS domain. More particularly, there is a need for blocking and unblocking I/O traffic for selected physical or logical devices connected to a common SAS expander or initiator.

SUMMARY

The invention provides a SAS expander with I/O control register bits within Phys associated with physical or logical I/O devices. Setting and unsetting the I/O control register bit for the Phy associated with a particular physical or logical device allows I/O traffic to be blocked and unblocked, as desired, to the selected physical or logical device. For example, a register bit setting of 0 may be used to enable OPEN requests, and a register bit setting of 1 may be used to disable OPEN requests. In a particular embodiment, when the register bit is set to a blocking state, an OPEN request that comes in on the SAS link is rejected using an OPEN_REJECT (RETRY) response.

An extension of the invention uses multiple I/O control register bits for each Phy so that individual protocols may be enabled and disabled independently for selected physical devices. For instance, register bits can be provisioned to reject SSP and STP/SATA requests, but to allow SMP OPEN requests. Each Phy may have its own set of enabled and disabled SAS protocols. In addition, each Phy may be configured the same as, or differently from, the other Phys in the SAS domain, as desired.

A related extension provides the ability to reject only those OPEN requests that attempt to go out of a SAS link. A use case for this capability may be to allow OPEN requests to travel inside of an expander (the defined SAS link for this purpose) but not to leave it. This allows the expander's bus agent to still send requests to the drive, but prevents the drive from interfering with the larger SAS domain for the period of time when the blocking bit is set. This capability may also be extended to SAS connection requests generally such that each Phy may have certain SAS protocols enabled, disabled, and/or disabled only for SAS protocols that attempt to leave a defined SAS link, as desired. Another related extension is to selectively ORR (OPEN_REJECT (RETRY)) a request to open a SAS connection or the use of a particular SAS address received in response to the setting of associated bits.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not necessarily restrictive of the invention as claimed. The accompanying drawings,

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which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and together with the general description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE FIGURES

The numerous advantages of the invention may be better understood with reference to the accompanying figures in which:

FIG. 1 is a functional block diagram of a host computer and SAS expander using register bits to control I/O traffic from selected physical devices.

FIG. 2 is a functional block diagram of a method for using register bits to control I/O traffic from selected physical devices.

FIG. 3 is a functional block diagram of a host computer and SAS expander using register bits to control I/O traffic for specific SAS Requests received from selected physical devices.

FIG. 4 is a functional block diagram of a method for using register bits to control I/O traffic for specific SAS Requests received from selected physical devices.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The invention may be embodied in a SAS expander with register bits for Phys associated with physical or logical I/O devices. While the disclosure positions the I/O control register bits at the Phy level, it will be understood that the I/O control register bits could be located in any SAS I/O mediation device and at any desired level in the SAS domain. Nevertheless, locating the I/O control register bits at the Phy level within the SAS expander is advantageous and will be described as an illustrative, but not the exclusive, embodiment of the invention.

The invention may be, but is not limited to, providing a mechanism within a SAS expander to selectively enable and disable incoming or outgoing OPEN requests for a selected physical or logical device. In a particular embodiment, the invention may be part of the SAS expander link in which setting and unsetting a register bit in the Phy associated with a particular physical or logical device allows I/O traffic to be blocked and unblocked, as desired, to the selected device. By way of example, I/O traffic may be selectively blocked and unblocked to any physical device, logical device, another SAS expander, or any other desired SAS target served by the SAS expander. For example, a register bit setting of 0 may allow OPEN requests, and a register bit setting of 1 may reject OPEN requests. When enabled for this example, an OPEN request that comes in on the SAS link is rejected using OPEN_REJECT (RETRY).

SAS agents, including initiators, expanders and targets contain SAS Phys, which provide the low-level communication interface between these devices. The SAS Phy is a combination of the physical or logical device layer, phy layer and link layer functions. A minimum of two Phys (one at each end point) is typically required to complete a SAS physical or logical connection pathway. The placement of the I/O "OPEN reject" register bit at the SAS Phy level is advantageous to the operation of the system in order to prevent rejected OPEN requests from entering the connection manager's hardware state machine. This characteristic allows OPEN requests to be rejected for a selected physical device while allowing I/O flow to continue on any links where the "OPEN reject" capability is not enabled. As a result, important processes, such as