SEMICONDUCTOR DIE PACKAGE WITH REDUCED INDUCTANCE AND REDUCED DIE ATTACH FLOW OUT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is generally in the field of semiconductors. More specifically, the invention is in the field of semiconductor packaging.

2. Related Art

During semiconductor packaging, dice are mounted onto a die attach pad fabricated on a substrate surface. A die adhesive is commonly used to attach the die to the die attach pad. For example, epoxy resin is a common type of die attach adhesive used for this purpose. Such epoxies can be referred to as "die attach epoxies." After the die is mounted on the substrate, bond wires are used to electrically connect die wire bond pads located on the die to their corresponding substrate ground pads and substrate signal pads located on the substrate.

In general, it is desirable to reduce the length of the bond wires used to connect the die wire bond pads to the substrate ground pads and substrate signal pads. A significant advantage, for example, is the reduced inductance of shorter bond wires. On the other hand, inductance in a bond wire increases as the length of the bond wire increases. Dice comprising power amplifier devices are particularly sensitive to the length of the bond wire used to connect a die wire bond pad to a substrate ground pad, and can thus greatly benefit from reduced bond wire lengths. Other advantages associated with shorter bond wires include reduced package sizes and reduced manufacturing costs, both of which are desirable.

However, due to a number of factors, the amount of reduction that can be made to the length of bond wires is extremely limited. For example, when the die is attached to the die attach pad using die attach adhesive, the die attach adhesive naturally flows out beyond the bottom surface of the die and partially extends into the substrate ground pad area. This "flow out" of die attach adhesive extends the distance between the die and the location on the substrate pad to which a bond wire may be attached. This extended distance corresponds to increased bond wire length for connecting the die wire bond pad to the substrate pad.

Longer bond wire lengths may also be required due to the design of the die. For example, as the thickness of the die increases, longer bond wires become necessary. Furthermore, the location of the wire bond pad on the die may also dictate the length of the bond wire required. For example, as wire bond pads are moved away from the edge of the die toward the center of the die, longer bond wires are required.

Accordingly, there is a strong need in the art for a structure and technique which reduces the length of bond wires connecting die wire bond pads to substrate ground pads and/or substrate signal pads during semiconductor die packaging. Furthermore, there is a need in the art for a structure and technique for controlling die attach adhesive flow out during semiconductor die packaging.

SUMMARY OF THE INVENTION

The present invention is directed to a semiconductor die package with reduced inductance and reduced die attach adhesive flow out. The invention overcomes the need in the

art for reducing the length of bond wires and the need in the art for controlling die attach adhesive flow out in semiconductor die packaging.

In one exemplary embodiment, a structure comprises a substrate having a top surface, and a die attach pad situated on the top surface of the substrate. The die attach pad includes a die attach region and at least one substrate ground pad region electrically connected to the die attach region. The die attach pad further includes a die attach stop between the die attach region and the at least one substrate ground pad region. The die attach stop acts to control and limit die attach adhesive flow out to the at least one substrate ground pad region during packaging so that the at least one substrate ground pad region can be moved closer to the die attach region so that shorter bond wires for connecting the at least one substrate ground pad region to a die wire bond pad may be used during packaging.

According to one particular embodiment, the die attach stop comprises an opening defined in the die attach pad between the die attach region and the at least one substrate ground pad region. A depth of the opening may be, for example, approximately equal to a height of the die attach pad. A heat spreader may further be situated on a bottom surface of the substrate. Vias in the substrate provide a connection between the at least one substrate ground pad region and the heat spreader.

According to another particular embodiment, the die attach stop comprises a dam situated over and electrically coupled with the at least one substrate ground pad region. The dam includes a top surface and a wall, wherein the wall extends from the top surface of the dam to the at least one substrate ground pad region. A heat spreader may further be situated on a bottom surface of the substrate. Vias in the substrate provide a connection between the at least one substrate ground pad region and the heat spreader.

According to various embodiments of the invention, greater control of die attach adhesive flow out during semiconductor packaging is achieved and, as a result, length of bond wires can be reduced, which leads to reduced inductance. Furthermore, package size can be reduced, and manufacturing costs are also reduced. Other features and advantages of the present invention will become more readily apparent to those of ordinary skill in the art after reviewing the following detailed description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a cross-sectional view of a known semiconductor die packaging structure.

FIG. **2**A illustrates a cross-sectional view of an exemplary structure in accordance with one embodiment of the present invention.

FIG. **2**B illustrates a top view of the exemplary structure of FIG. **2**A.

FIG. **3** illustrates a cross-sectional view of an exemplary structure in accordance with one embodiment of the present invention.

FIG. **4** illustrates a cross-sectional view of an exemplary structure in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to a semiconductor die package with reduced inductance and reduced die attach