



(12) **United States Patent**  
**Bhatia et al.**

(10) **Patent No.:** **US 9,411,391 B2**  
(45) **Date of Patent:** **Aug. 9, 2016**

(54) **MULTISTAGE LOW LEAKAGE ADDRESS DECODER USING MULTIPLE POWER MODES**

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(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 52 days.

(21) Appl. No.: **14/269,841**

(22) Filed: **May 5, 2014**

(65) **Prior Publication Data**

US 2015/0227186 A1 Aug. 13, 2015

**Related U.S. Application Data**

(60) Provisional application No. 61/937,029, filed on Feb. 7, 2014.

(51) **Int. Cl.**

**G06F 1/32** (2006.01)  
**G11C 5/14** (2006.01)  
**G06F 12/06** (2006.01)  
**G06F 12/02** (2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ..... **G06F 1/3203** (2013.01); **G06F 12/0223** (2013.01); **G06F 12/06** (2013.01); **G11C 5/14** (2013.01); **G11C 5/147** (2013.01); **G11C 7/1096** (2013.01); **G11C 11/419** (2013.01); **G06F 2212/1016** (2013.01)

(58) **Field of Classification Search**

CPC ... G06F 1/3203; G06F 12/06; G06F 12/0223; G06F 2212/1016; G11C 5/14; G11C 7/1096; G11C 5/147; G11C 11/419

See application file for complete search history.

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(57) **ABSTRACT**

A system and method for managing power in a memory, wherein the system may include a processor and a memory unit coupled to the processor. The memory unit may initialize an address decoder into a first power mode. In response to receiving a command and an address corresponding to a location within the memory unit, the memory unit may use the first stage of the address decoder to decode at least a portion of the address. The memory unit may further switch a selected portion of a second stage of the address decoder from the first power mode to the second power mode, wherein the selected portion of the second stage of the address decoder is selected dependent upon an output signal of the first stage of the address decoder.

**20 Claims, 16 Drawing Sheets**

