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(54) **SOLID-STATE IMAGING DEVICE AND METHOD FOR DRIVING THE SAME**

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(58) **Field of Classification Search** 257/146, 257/202, 291, 428, 431, 432, E31.001; 438/129, 438/48, 65

See application file for complete search history.

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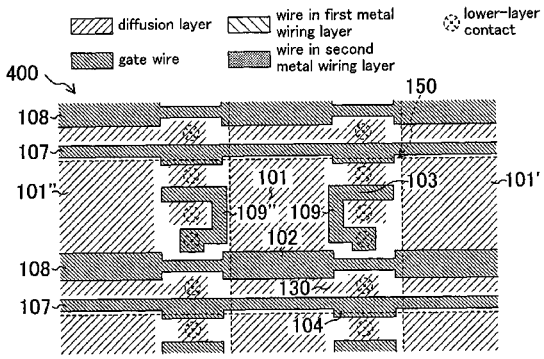
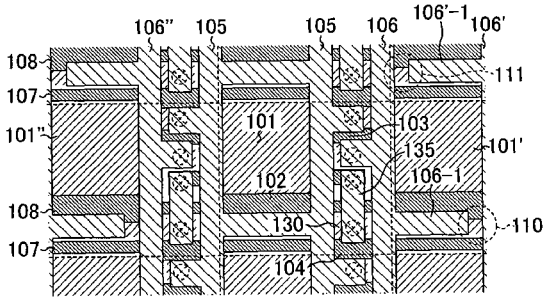
(57) **ABSTRACT**

A pixel array is provided in which cells are arranged in a matrix. Each cell includes a photodiode, an FD, a transfer transistor, a reset transistor, an amplifying transistor having a gate electrode connected to the FD, a drain connected to a power supply line, and a source connected to a vertical signal line, and an FD wire. The FD wire is provided in a first wiring line, and the vertical signal line is provided in a second wiring line positioned over the first wiring layer. Since the potential of the FD wire follows the potential of the vertical signal line, it is possible to suppress a variation in capacitance occurring in the FD when a position of the vertical signal is shifted, depending on a position of the cell.

14 Claims, 32 Drawing Sheets