THREE-TERMINAL POWER MOSFET SWITCH FOR USE AS SYNCHRONOUS RECTIFIER OR VOLTAGE CLAMP

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of application Ser. No. 08/648,266, filed May 15, 1996, now U.S. Pat. No. 5,744,994.

This application is related to application Ser. No. 08/648,334, filed May 15, 1996, now U.S. Pat. No. 5,818,084, and application Ser. No. 08/649,747, filed May 15, 1996, now U.S. Pat. No. 5,689,144, each of which is being filed concurrently herewith and is incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

This invention relates to power MOSFET switches for use as a synchronous rectifiers or voltage clamps in power converters and other circuits.

BACKGROUND OF THE INVENTION

Semiconductor devices are frequently used to switch currents in power electronic circuits. These devices normally contain PN junctions or diodes which can be driven into forward conduction or into avalanche breakdown by any voltage spikes which occur in the circuit. One common type of switching device, for example, is the power MOSFET, which has been discussed extensively in the literature since about 1980. Any MOSFET which has a normal source-body short contains a parasitic PN diode at the junction between its drain and body regions. The parasitic diode is often referred to as an "anti-parallel" diode since it is parallel to the current path through the channel of the MOSFET but is oriented such that it is normally reverse-biased.

The anti-parallel diode in a power MOSFET can become forward-biased in several ways. For example, an electrostatic discharge (ESD) in the circuit may cause this to happen. Moreover, in numerous power electronic circuits, an inductance in a path of large current flow produces rapid changes in voltage across its terminals as the inductance attempts to resist any changes in the magnitude of the current flowing through it. The well-known equation $V_L=L\ dI/dt$ describes this phenomenon and indicates that decreasing the current in an inductor, or opening a switch in series with an inductor, produces a negative value of V_L, i.e., a reversal in the polarity of the voltage across its terminals. If the magnitude of the reversed voltage exceeds the supply voltage, any number of circuit connections (customarily referred to as "nodes" in circuit theory) can reach potentials which are outside the range of the power supply voltage. In these instances, the anti-parallel PN diode in the MOSFET switch can become temporarily forward-biased.

In a motor driver, for example, shutting off a MOSFET that is connected in series with any of the motor windings will cause inductive flyback. In a push-push (i.e., halfbridge) driver, two switches are stacked one over the other between the supply rails, with the centerpoint between the switches connected to the motor. Generally, the high-side switch is turned on when the low-side switch is turned off, and vice-versa. In reality, however, the MOSFETs cannot be switched simultaneously because of the risk of overlapping on-states, which would produce a catastrophic current "shoot through" between the supply rails. Therefore, it is

customary to provide a short "break-before-make" interval between the turn-off of one switch and the turn-on of the other switch, often referred by as a tri-state. Thus, following the turn-off of the low-side switch (with the high-side switch still turned off) the motor winding will drive the output (centerpoint) to a voltage above the positive rail and forward-bias the anti-parallel diode in the high-side MOSFET; and conversely, following the turn-off of the high-side switch (with the low-side switch still turned off) the motor winding will drive the output to a voltage below ground and forward-bias the anti-parallel diode in the low-side MOSFET. In other words, during the tri-state the inductive load will necessarily forward-bias one of the two anti-parallel diodes in the halfbridge. Conduction in the anti-parallel diodes is unavoidable.

In other circuits, such as those used in switching-mode DC-DC convertors and other power supplies, the anti-parallel diodes in the switching MOSFETs are intentionally made to conduct. In these circuits, the MOSFET is connected directionally in the manner of a rectifier so as to allow its parasitic diode to conduct whenever the "switch" of the converter is opened. The gate of the MOSFET is synchronized to cause the MOSFET to shunt current from its diode (through its channel) whenever the anti-parallel diode is forward-biased. Hence, the MOSFET is often described as a "synchronous rectifier". Once again, however, a make-before-break interval is required between the time when the parasitic diode begins to conduct and time when the gate of the MOSFET is driven to turn the channel of the MOSFET on. During the break-before-make interval, the gate of the MOSFET is biased so as to turn the channel off.

Accordingly, as a general rule in this type of circuit, an interval must exist during which the parasitic PN diode in the MOSFET is conducting and before the MOSFET (or some other MOSFET in the circuit) is turned on to divert the current flow from the diode to a channel. Parasitic diode conduction cannot be avoided in most inductive power circuits.

When forward-biased, a PN diode is a minority carrier device and, as such, has a long recovery time compared to majority carrier devices. While the PN diode is forward-biased, minority carriers are stored in the PN diode. In the event that the PN diode once again becomes reverse-biased, the stored minority carriers increase the reverse recovery time of the PN diode (i.e., the time it takes a forward-biased diode to block a voltage applied in the reverse direction). Furthermore, once the minority carriers are removed under reverse-bias, a rapid voltage transient (i.e., large dv/dt) will occur, and voltage spikes beyond the supply voltages may also occur.

This same phenomenon applies to the anti-parallel diode within a MOSFET and can degrade the performance of the MOSFET should its parasitic PN diode become momentarily forward-biased. During the operation of an N-channel MOSFET in Quadrant I (where the source terminal is connected to a lower voltage than the drain terminal), the parasitic diode is reverse-biased and will conduct no current. However, if the MOSFET should operate in Quadrant III (where the source terminal is connected to a higher voltage than the drain terminal), the parasitic diode will become forward-biased and will conduct a current with minority carriers. (Note. Unless otherwise specified herein, in MOSFETs where the body is shorted to a drain/source terminal, the shorted terminal will be referred to as the "source" and the non-shorted terminal will be referred to as the "drain". In instances where the terms source and drain relate to their electrical function rather than their structure, the term "elec-