

Referring initially to FIGS. 1 and 2, an electronic still camera 1 is divided generally into an input section 2 and an interpolation and recording section 4. The input section 2 includes an exposure section 10 for directing image light from a subject (not shown) toward an image sensor 12. Although not shown, the exposure section 10 includes conventional optics for directing the image light through a diaphragm, which regulates the optical aperture, and a shutter, which regulates exposure time. The image sensor 12, which includes a two-dimensional array of colored photosites or pixels corresponding to picture elements of the image, can be a conventional charge-coupled device (CCD) using either well-known interline transfer or frame transfer techniques. The image sensor 12 is covered by a color filter array (CFA) 13. For an example of a color filter array which is particularly suitable for use in the present invention reference is made to commonly-assigned U.S. Pat. No. 5,631,703 to Hamilton et al, the disclosure of which is incorporated by reference. The image sensor 12 is exposed to image light so that analog image charge information is generated in respective photosites. The charge information is applied to an output diode 14, which converts the charge information to analog image signals corresponding to respective picture elements. The analog image signals are applied to an A/D converter 16, which generates a digital image value from the analog input signal for each picture element. The digital values are applied to an image buffer 18, which may be a random access memory (RAM) with storage capacity for a plurality of still images.

A control processor 20 generally controls the input section 2 of the electronic still camera 1 by initiating and controlling exposure (by operation by the diaphragm and shutter (not shown) in the exposure section 10), by generating the horizontal and vertical clocks needed for driving the image sensor 12 and for clocking image information therefrom, and by enabling the A/D converter 16 in conjunction with the image buffer 18 for each value segment relating to a picture element. The control processor 20 typically includes a microprocessor and appropriate memory coupled to a system timing circuit. Once a certain number of digital image values have been accumulated in the image buffer 18, the stored values are applied to a digital signal processor 22, which controls the throughput processing rate for the interpolation and recording section 4 of the electronic still camera 1. The digital signal processor 22 applies an interpolation algorithm to the digital image values, and sends the interpolated values to a conventional, removable memory card 24 via a connector 26. Although an electronic still camera 1 has been described as including a digital signal processor, it will be understood that the digital signal processor 22 does not have to be an integral part of the electronic still camera 1. A requirement of this invention is that the digital image values are provided from an image sensor.

Since the interpolation and related processing ordinarily occurs over several steps, the intermediate products of the processing algorithm are stored in a processing buffer 28. The processing buffer 28 may also be configured as part of the memory space of the image buffer 18. The number of image values needed in the image buffer 18 before digital processing can begin depends on the type of processing, that is, for a neighborhood interpolation to begin, a block of values including at least a portion of the image values comprising a video frame must be available. Consequently, in most circumstances, the interpolation may commence as soon as the requisite block of picture elements is present in the buffer 18.

The input section 2 operates at a rate commensurate with normal operation of the electronic still camera 1 while interpolation, which may consume more time, can be relatively divorced from the input rate. The exposure section 10 exposes the image sensor 12 to image light for a time period dependent upon exposure requirements, for example, a time period between $\frac{1}{1000}$ second and several seconds. The image charge is then swept from the photosites in the image sensor 12, converted to a digital format, and written into the image buffer 18. The driving signals provided by the control processor 20 to the image sensor 12, the A/D converter 16 and the buffer 18 are accordingly generated to achieve such a transfer. The processing throughput rate of the interpolation and recording section 4 is determined by the speed of the digital signal processor 22.

One desirable consequence of this architecture is that the processing algorithm employed in the interpolation and recording section may be selected for quality treatment of the image rather than for throughput speed. This, of course, can put a delay between consecutive pictures which may affect the user, depending on the time between photographic events. This is a problem since it is well known and understood in the field of electronic imaging that a digital still camera should provide a continuous shooting capability for a successive sequence of images. For this reason, the image buffer 18 shown in FIG. 1 provides for storage of a plurality of images, in effect allowing a series of images to "stack up" at video rates. The size of the buffer is established to hold enough consecutive images to cover most picture-taking situations.

An operation display panel 30 is connected to the control processor 20 for displaying information useful in operation of the electronic still camera 1. Such information might include typical photographic data, such as shutter speed, aperture, exposure bias, color balance (auto, tungsten, fluorescent, daylight), field/frame, low battery, low light, exposure modes (aperture preferred, shutter preferred), and so on. Moreover, other information unique to this type of electronic still camera 1 is displayed. For instance, the removable memory card 24 would ordinarily include a directory signifying the beginning and ending of each stored image. This would show on the display panel 30 as either (or both) the number of images stored or the number of image spaces remaining, or estimated to be remaining.

The digital signal processor 22 interpolates each still video image stored in the image buffer 18 according to the interpolation technique shown in FIG. 2. The interpolation of missing data values at each pixel location follows the sequence shown in FIG. 2, as will later be discussed.

In the implementation shown in FIG. 2, the digital signal processor 22 provides an adaptive interpolation technique to provide a compute luminance function shown as luminance values block 32 for optimizing luminance values as will be described hereinafter in connection with FIG. 3A. After the luminance values are computed then a chrominance values block 34 computes the chrominance values of each pixel based upon the computed final luminance values. Finally an RGB values block 36 computes the image in Red(R), Green(G), Blue(B) format which are used for an image display or for making a hard copy output. Although this disclosure is in reference to computing red, green, and blue values, it will be understood that it is also applicable to other color spaces such as cyan, magenta, and yellow. Another color space that can be used is to use luminance and chrominance values which are typically referred to as YCC color spaces. The Y refers to luminance and the two C's refer to chrominance.