

in a similar way by the inverted control signal DF2 or DF2' available from terminal 29 over the readout control circuit (43) and the connection 64. The readout control circuit 43 is synchronized with the horizontal frequency pulse signal in FIG. 4.

The data read out of the buffer storage unit 41, either directly or through the D registers 45-50, are then supplied to the interpolator 46 designated by a rectangular broken-line enclosure 46 in FIG. 4, in the following manner. The luminance signals are supplied on the one hand directly and on the other hand through a D register 45 having a storage time of 1 pixel interval. The chrominance signals are read out into four D registers 47, 48, 49 and 50. Register 47 stores the last R-Y pixel value, register 48 the last B-Y value, Register 49 the first R-Y value and register 50 the first B-Y value. Undisturbed pixels go directly through the register 50 and the adding circuit 56 to the chrominance (C) output 5. The D-Registers are controlled so that either content of the register 47 or that of the register 48 and either the content of the register 49 or that of the register 50 are supplied to the interpolator 46. For the time slots of the interpolated pixel values designated I in FIG. 2 the necessary support values are prepared for the interpolator 46 in the D registers 45, 47, 48, 49 and 50, namely two support values for the luminance signal Y and four support values for the chrominance signal C.

The interpolator 46 consists essentially of a pair of subtraction stages 51 and 52, a pair of multiplier stages 53 and 54 and a pair of addition stages 55 and 56, as well as a coefficient control circuit consisting of a counter 57 and a programmable read-only memory (PROM) 58. The subtraction stages 51 and 52 each produce the difference between the pixel values supplied at their inputs and supply that difference to the corresponding multipliers 53 and 54, where they are weighted with the interpolation coefficients stored in the PROM 58, which are dependent on the size of the width of the defect (control signal DFW or DFW' at the terminal 31) and the state of the counter 57. For the duration of the defect location control signal DF2 or DF2', which is supplied from the terminal 29 through the propagation time equalizing circuit 59 to the counter 57, the content of the counter 57 increases at the data clock rate SCK of the luminance signal and the stored interpolation coefficients are called out in accordance with the counter content.

The weighted difference signals at the output of the multiplier stages 53 and 54 are respectively supplied to first inputs of the addition stages 55 and 56, at the respective second inputs of which another signal corresponding to the next pixel is applied. At the outputs 4 and 5 of the interpolator 46, there are, in some cases, signals of undisturbed pixels, resulting from a null interpolation coefficient supplied by the PROM 58 and, in some cases, interpolated pixel signals derived from undisturbed pixel signals.

FIG. 5 illustrates, in a manner similar to FIG. 2, but adapted to the processing described in connection with FIG. 4, the case of a signal in which a defect extending over four adjoining pixels is detected. This is shown for only horizontal pixel sequences.

The first line shows a modified defect location signal which appears on the connection line 64 in FIG. 4.

The second line shows the read-out from the FIFO storage unit 41, with the pixel value 7 repeated during the interval covered by the defect.

The third line shows the content of the D register 45 for the pixel intervals which provide the common time scale of all of the lines of FIG. 5. The values "x" represent values that will not be used and therefore do not matter ("don't care values").

The fourth line of FIG. 5 shows the output of the multiplier 53 on the multibit line 62 between the multiplier 53 and the adder 55. In this case the multiplying factor, and therefore the product value, is 0 for the first two intervals shown and also for the last two whereas for the four in between the products are respectively 4/5 of the difference (2)-(7), 3/5, 2/5 and 1/5 of that difference.

On the fifth line of FIG. 5 is the output 4 of the adder 55 for the luminance signal Y, in which the first two and the last two intervals are occupied by the undisturbed values appearing in those intervals in the second line of FIG. 5. The interpolated values now become 4/5 of 2+1/5 of 7, 3/5 of 2+2/5 of 7, 2/5 of 2+3/5 of 7 and 1/5 of 2+4/5 of 7.

The sixth through the twelfth lines of FIG. 5 illustrate the processing of the chrominance signal. On the sixth line of FIG. 5 there appear alternately R-Y and B-Y signals abbreviated as R and B in FIG. 5, the circled numbers corresponding to the values of luminance signal shown in the second line of FIG. 5. The seventh line of FIG. 5 shows the content of the register 47. The values designated as "x", as in the case of the third line of FIG. 5, are "don't care" values, since they will not appear at the output of the processor.

The eighth line of FIG. 5 shows the content of the register 48, while the ninth and tenth lines of FIG. 5 respectively show the contents of the registers 49 and 50.

The eleventh line of FIG. 5 shows the output on the line 63 of the multiplier 54, which is 0 for the first three pixel intervals and for the last two, and, for the other four pixels, respectively $\frac{2}{3}$ and $\frac{1}{3}$ of the difference between R₁ and R₇ and $\frac{2}{3}$ and $\frac{1}{3}$ of the difference between B₁ and B₇. Finally, the twelfth line of FIG. 5 shows the chrominance signal which appears at the output 5 of the adder 56. The interpolated values that appear there are, respectively, $\frac{2}{3}R_1 + \frac{1}{3}R_7$, $\frac{2}{3}B_1 + \frac{1}{3}B_7$, $\frac{1}{3}R_1 + \frac{2}{3}R_7$ and $\frac{1}{3}B_1 + \frac{2}{3}B_7$ and are preceded by the undisturbed pixels R₁ and B₁ delayed by one chrominance pixel interval and are followed by more undisturbed chrominance pixels.

Although the invention has been described with reference to particular illustrated embodiments, it will be understood that variations and modifications are possible within the inventive concept.

We claim:

1. Method of concealing errors in a digital video signal by replacing disturbed pixel values with values derived from neighboring undisturbed pixel values, comprising the steps of:

detecting disturbed pixel values in a manner indicating pixel disturbance width (DFW) of a disturbance affecting values of a plurality of adjoining pixels in the same horizontal line as well as indicating pixel disturbance location (DF, DF1, DF2) of said pixels of affected value and

time-expanding the video signal of said same horizontal line outside of and adjacent to said plurality of adjoining pixels of said same line having disturbed values, by inserting in said video signal, between successive pixels of undisturbed value in said same line, interpolated pixel values derived from values