

picture line which is expanded (i.e., while inserting interpolated values less frequently).

Line c of FIG. 2 shows another advantageous variant of the expansion of the undisturbed part of a video signal which has the same disturbed portion shown in line a of FIG. 2, but in this case the expansion factor rises, on account of the control signals DF2' and DFW' shown in lines e<sub>2</sub> and f<sub>2</sub> of FIG. 2, as the center of disturbance is approached (a first interpolated value lies between pixels 4 and 5, two additional interpolated values lie between pixels 5 and 6 and then five interpolated values between the pixels 6 and 18). After the center of the disturbances is passed the expansion factor decreases. In this method the transition between the values on the edges of the disturbance region (pixels 6 and 18) is smoother and the expanded picture area includes only a narrow strip on each side of the defective area covered.

The video signals made available at the outputs 4 and 5 are, as shown in FIG. 1, furnished in parallel to two signal branches. On the one hand, they proceed, through a delay circuit 7 for equalizing the propagation time of the other branch, to the first input of a first fader 8 and, on the other hand, they go through a "horizontal" low pass filter 9 which is variable in its cut-off frequency and then to the second input of the first fader 8. Faders are well known devices for fading one picture in while another is faded out either in space (blending in an insert) or in time (fading in a new scene).

The output of the first fader 8 is also split, going on the one hand through a second propagation time equalizing delay 11 to a first input of a second fader 12 and on the other hand going through a "vertical" low pass filter 13 of variable cut-off frequency and then to a second input of the second fader 12. The fading time of the faders 8 and 12 for fading between the first and second inputs is in each case of about the duration two intervals at which successive pixels arrive. The low pass filtering which is produced respectively in the horizontal and in the vertical direction is of value for improving the viewer's impression of the picture in the neighborhood of the detected defect. Such filtering of digital video signals is a known technique (which usually involves non-recursive digital filtering) and the provision of digital filters of variable order (i.e. of variable cut-off frequency) is illustrated in U.S. Pat. No. 4,488,251.

The cut-off frequencies of the filters 9 and 13 are dependent upon the geometric dimensions of the detected defect. The vertical low pass filter 13 particularly improves the reproduction of diagonal picture structures. An extensively improved video signal composed of a luminance signal Y and a chrominance signal C, both corrected over the defect location, is accordingly obtainable at the outputs 14 and 15 of the second fader 12. The faders fade in the corrected signals in filtered form in the region of the detected defect, under control of a signal generated in the circuit 6 which controls both the variable filter and the fader, as shown by the connections of the control signals LPFV and LPFH in FIG. 1.

The generation of control signals for the video signal processing for concealing defect locations is further explained with reference to the circuit block diagram of FIG. 3. The defect location signal DF available at the terminal 21 is typically of a kind produced in known devices for recognition of scratches or dust specks on a film being processed by a film scanner of a television broadcast station or television studio. Subjecting the

signal DF to a simple delay by means of the propagation time equalizing stage 22 produces the delayed defect location signal DF1 shown on line d of FIG. 2, which is available at the output 23 at the lower left of FIG. 3. The defect location signal DF is also supplied immediately to a circuit 24 for indication of the width of the defect by a suitable signal. This width information supplied by the multibit output of the recognition circuit 24 is stored in a FIFO defect location storage unit 26, which is also supplied with the inverted defect location signal  $\overline{DF}$  obtained through an inverter 25. The delayed defect location signal DF1 is also supplied to the FIFO storage unit 26.

A circuit 27 for recognizing the spacing between defect locations is also provided, to which there are supplied both the defect location system signal DF and the delayed defect location signal DF1 produced by the delay circuit 22. This circuit measures the interval between successively detected defect locations and provides that information for the next circuit to be described, which is the expansion and low pass filtering control signal generator 28. The latter circuit also receives the defect width information from the FIFO storage unit 26. From these inputs the circuit 28 produces a defect location control signal DF2 or DF2' furnished to terminal 29 and a related width information signal DFW or DFW' supplied at the output 31. The pulses DF2' can be generated by a circuit including a counter and a PROM so that the sum of the lengths of these pulses (line e<sub>2</sub> of FIG. 2) is equal to the length of the defect location pulse DF1 (line d of FIG. 2). That relation also holds true for the pulses DF2 (line e<sub>1</sub> of FIG. 2) which provide broader expansion. The information regarding the spacing between successive defect locations is important and necessary, because the width of the wider-than-defect location covered by the processing depends thereon. The smaller the spacing between the defects is found to be, the shorter the "expansion" of the defect location carried out by processing must be.

The circuit 28 also generates the fading control signals LPFH and LPFV (supplied respectively at terminals 32 and 33) for fading in and out the filtered video signals produced by the horizontal and vertical low-pass filters 9 and 13. Horizontal scanning frequency pulse signals are supplied to the storage unit 26 and to the control circuit 28 respectively over terminals 34 and 35 for synchronization with the television line rhythm. The reading out from the FIFO storage unit 26 is produced by the delayed defect location signal DF1. The output signals of the expansion control signal circuit 28 are correlated with DF1 in the manner illustrated in FIG. 2.

FIG. 4 shows a block circuit diagram corresponding to the unitary unit block 3 shown in FIG. 1 for the video signal processing. Those components already identified in the foregoing which also appear in FIG. 4 are given the same reference numerals in FIG. 4. The luminance signal Y and the chrominance C are supplied over the lines 1 and 2 to a buffer storage unit 41 in which, however, only the undisturbed pixels are stored as a result of control of the write-in pulses by means of the signal DF1 from the terminal 23. The clock signals SCK and the delayed defect signal DF1 go to the AND circuit 42, which provides a clock signal output only when DF1 is at its low value. The small circle at one input of the AND circuit 42 designates inversion of DF1 there. The reading out of the stored pixel values is controlled