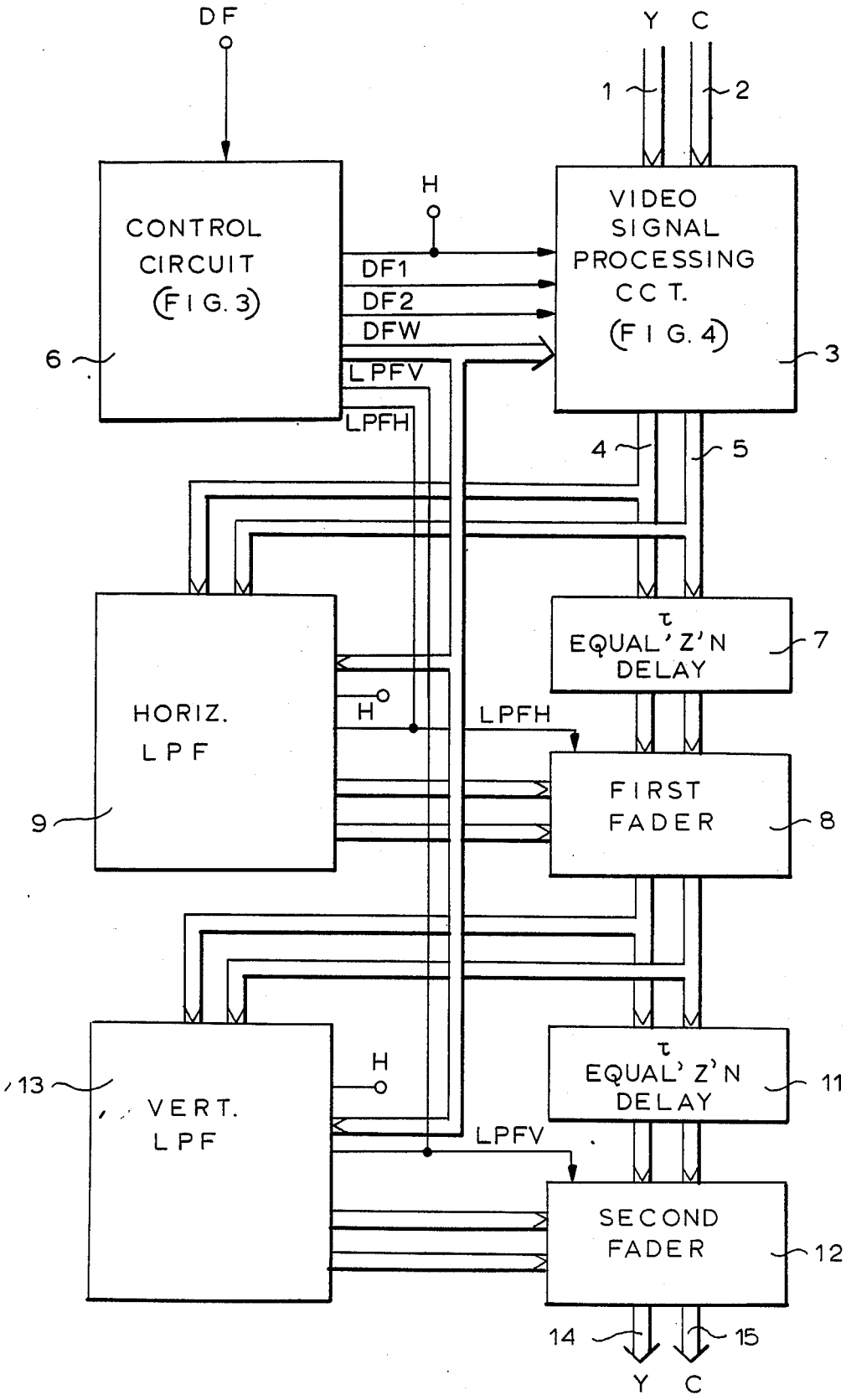
FIG. 1


DF
Y C
1
2
CONTROL CIRCUIT (FIG. 3)
6
H
DF1
DF2
DFW
LPFV
LPFH
VIDEO SIGNAL PROCESSING CCT. (FIG. 4)
3
4
5
τ EQUAL'Z'N DELAY
7
HORIZ. LPF
9
H
LPFH
FIRST FADER
8
13
VERT. LPF
H
LPFV
τ EQUAL'Z'N DELAY
11
SECOND FADER
12
14
15
Y C