

said chrominance signal output of said buffer storage means through said second and third D registers (47, 48) and having a second input connected to said chrominance output of said buffer storage means through said fourth and fifth D registers (49,50), said fourth and fifth D registers having means for providing buffer storage therein for a period exceeding the storage period in said second and third D registers by one pixel arrival interval;

a PROM (58) wherein multiplying factors for interpolation are stored;

first and second multipliers stages (53, 54) respectively having first inputs respectively connected to the outputs of said first and second subtraction stages (51, 52) and having second inputs connected to the output of said PROM (58) wherein multiplying factors for interpolation are stored;

counting means (57) controlled by said defect location control signal (DF2, DF2') for controlling said PROM (58);

first and second addition stages (55, 56), said first addition stage 55 having a first input connected to the output of said first multiplier (53) and a second input connected to said luminance signal output of said buffer storage means (41) and having an output for providing expanded luminance signals and said second addition stage (56) having a first input connected to the output of said second multiplier (54) and a second input connected to the output of said fourth and fifth D registers and having an output for providing expanded chrominance signals, and D register control means responsive to said defect location control signal, responsive to clock signals which are also used for advancing said counting

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means (57) and synchronized to synchronizing signals of a scanning frequency of said digital video signals, for timing the operation of said first to fifth D registers and for selectively operating simultaneously either of said second and fourth D registers or said third and fifth D registers.

11. The apparatus as defined in claim 10 comprising also horizontal low pass digital filter means, vertical low pass digital filter means, first signal fader-blender means (8) and second signal fader-blender means (12) and means responsive to said defect location signal (DF1) for controlling said digital filter means with respect to their cut-off frequency and for controlling said fader-blender means for substituting digital filter output signals for input signals not subjected to digital filtering, and first and second propagation time equalizing delay means, said first fader-blender means (8) having first inputs connected through said first propagation time equalizing time delay means respectively to said outputs of said first and second addition means, and having second inputs connected respectively to said outputs of said first and second addition means (55, 56) through said horizontal direction digital filter means (9), said second fader-blender means (12) having first inputs connected through said second propagation time equalization delay means (11) respectively to outputs of said first fader-blender means (8) and second inputs connected through said vertical direction digital filter means (13) respectively to said outputs of said first fader-blender means (8), said second fader blender means (12) having outputs respectively providing luminance and chrominance signals for further transmission and/or processing.

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