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(54) **CLOCK GENERATION DEVICE AND SEMICONDUCTOR DEVICE INCLUDING THE SAME**

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(52) **U.S. Cl.**
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(58) **Field of Classification Search**
None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,931,986 A * 6/1990 Daniel G06F 1/10 327/261
6,750,692 B2 6/2004 Jang
7,266,743 B2 * 9/2007 Athavale G01R 31/318594 714/726
7,304,523 B2 * 12/2007 Yen H03L 7/113 327/160
8,183,905 B2 * 5/2012 Chang H03B 5/368 327/291
8,610,479 B2 * 12/2013 Lee H03L 7/22 327/113
8,841,960 B2 9/2014 Cho et al.
8,918,667 B2 * 12/2014 Ware G11C 7/04 710/61
9,244,485 B1 * 1/2016 Koh G06F 1/08
9,344,065 B2 * 5/2016 Ying H03K 3/013
9,495,231 B2 * 11/2016 Gilda G06F 1/12

* cited by examiner

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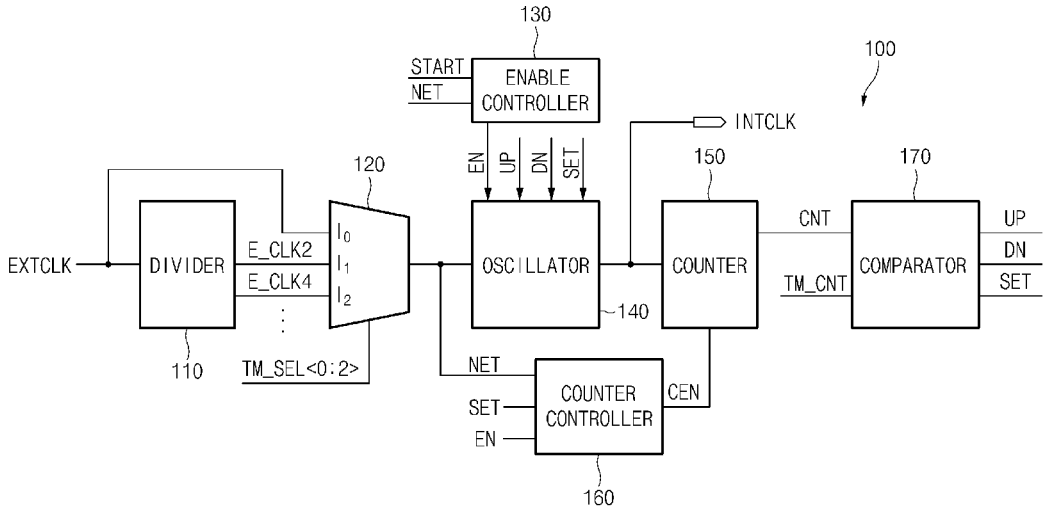
(57) **ABSTRACT**

A clock generation device and a semiconductor device including the same are disclosed, which may tune an internal clock to a desired frequency. The clock generation device may include an oscillator configured to tune an oscillation signal in response to a tuning signal, and adjust a period of an internal clock. The clock generation device may include a counter configured to count the internal clock in response to a count enable signal, and output a count signal. The clock generation device may include a comparator configured to compare the count signal with a test count signal including a target count number of the internal clock, and output the tuning signal.

26 Claims, 6 Drawing Sheets