(or fins) of a first semiconductor material such as silicon. The segments are integral with the wafer in which they are formed, are substantially parallel to one another, and advantageously are spaced apart by approximately the minimum line-width achievable with the technology used to form them.

The thin segments have first and second opposing major surfaces and, illustratively are identical to those that would be formed in making conventional finFETs. While the first and second opposing major surfaces are often illustrated as being parallel to each other, it will be understood that process limitations often result in a structure in which the first and second major surfaces slope outwardly from top to bottom of the segment so that the cross-section of the segment is trapezoidal in shape.

There are numerous ways to form the fins of a FinFET. Illustratively, a plurality of parallel, spaced-apart linear elements are formed on the surface of the silicon wafer where the finFETs are to be formed. Illustratively, the linear elements are dummy gate structures. The linear elements are approximately rectangular in cross-section and have a width that is approximately the desired spacing between adjacent fins of the finFET. Typically, this spacing is the minimum line-width achievable.

Spacers are then formed on the sides of the linear elements. Illustratively, a layer of appropriate material such as silicon nitride is deposited on the linear elements and the exposed surface of the silicon; and this layer is then anisotropically etched to remove all of the deposited layer down to the upper surfaces of the linear elements and the silicon except for narrow spacer regions on the sides of the linear elements.

The resulting structure is shown in the cross-section FIG. **6**A which depicts a silicon substrate **610**, linear elements **620** and spacers **630**. Advantageously the width of the linear elements **620** is approximately the minimum line-width achievable by the technology used to form the linear elements. The width of the spacers is considerably smaller than the width of the linear elements.

The same structure is shown in FIG. **7**A which depicts a silicon substrate **710**, linear elements **720**, and spacers **730** used in forming another embodiment of the invention.

The linear elements are then removed, thereby exposing the semiconductor material between the spacers. The spacers are then used in step **520** as hard masks in an etching process that removes the semiconductor material except for the material underlying the spacers, thereby forming channels in the semiconductor material that define a plurality of fins. The resulting structure as shown in FIG. **6**B comprises silicon wafer **610**, fins **640** which are capped by spacers **630** and channels **650** between fins **640**. FIG. **7**B similarly comprises silicon wafer **710**, fins **740** which are capped by spacers **730** and channels **750** between fins **740**.

The trapping regions are then formed. Where the trapping regions are doped implants, both p-type and n-type implants are typically formed in the same device. To do this, at step **530**, regions where the n-type implants are not to be made are masked off and the n-type implants are then made in the substrate as shown in FIG. **6**C. The resulting structure comprises wafer **610**, fins **640**, spacers **630**, channels **650**, and n-type implant regions **660** in the substrate between fins **640**. This process is then repeated at step **540** for the p-type implant. Regions where the p-type implants are not to be made are masked off and the p-type implants are then made. The resulting structure is the same as that shown in FIG. **6**C except that the implants in the substrate are p-type.

The spacers are then removed from the tops of fins **640** as shown in FIG. **6**D. And a field oxide is then formed at step **550** on top of the trapping region.

The finFETs are then completed by forming one or more gates on the fins at step **560**; and the gate is used as a mask for another ion implantation at step **570** that dopes the fins to form source and drain regions.

Where the trapping regions are doped epitaxial regions, both p-type and n-type epitaxial regions are typically formed in the same device. To do this, the spacers at the tops of fins **740** are removed as shown in FIG. **7**C. Then, at step **530**, regions where the n-type epitaxial regions are not to be grown are masked off and the n-type epitaxial regions are then grown as shown in FIG. **7**D. The resulting structure comprises wafer **710**, fins **740**, channels **750**, and n-type epitaxial regions **760** in the substrate between fins **740** as well as one the upper surfaces the fins. This process is then repeated at step **540** for the p-type implant. Regions where the p-type epitaxial regions are not to be grown are masked off and the p-type epitaxial regions are then grown. The resulting structure is the same as that shown in FIG. **7**D except that the epitaxial regions on the substrate are p-type.

A field oxide is then formed at step **550** on top of the trapping region; and the finFETs are completed as in steps **560** and **570**.

Where the trapping region is a high defect region, steps **530** and **540** are replaced by a single implantation step that forms all the trapping regions at once. Advantageously, this step is followed by a high temperature anneal. The resulting structure is similar to that shown in FIG. **6**E except that the implant regions **660** in substrate **610** are replaced by defect regions in the same location.

As will be apparent to those skilled in the art, numerous variations may be practiced within the spirit and scope of the present invention. For example, while the invention has been described in terms of forming finFETs in silicon wafers, numerous semiconductor materials may also be used in the practice of the invention such as germanium, gallium arsenide, indium phosphide, indium gallium arsenide and other III-V compounds. While one process has been described for the formation of the FinFETs, other processes may also be used; and numerous variations in these processes may also be practiced. Different materials may be used as cap layers, hard mask layers and spacers; and a wide variety of etchants and etching processes may be used to remove these materials. In the interest of brevity and to avoid obscuring the invention, many details of conventional processes for forming finFETs have been left out.

What is claimed is:

1. A finFET comprising:

a substrate of semiconductor material having a first conductivity type;

a plurality of first thin segments of the semiconductor material integral with the substrate and extending in a first direction away from the substrate, each first thin segment extending lengthwise in a second direction with a channel between adjacent thin segments;

a transistor formed on each of at least two adjacent first thin segments, each transistor having source and drain regions and a gate; and

at least one elongated trapping region located in or on the substrate between two adjacent first thin segments, the elongated trapping region having a second conductivity type opposite to the first conductivity type and being coupled to a well region having the second conductivity type.