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Tomassetti

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[54] METHOD FOR FABRICATING AN INTEGRATED BIPOLAR-CMOS CIRCUIT ISOLATION FOR PROVIDING DIFFERENT BACKGATE AND SUBSTRATE BIAS

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[*] Notice: The portion of the term of this patent subsequent to Mar. 27, 2007 has been disclaimed.

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Related U.S. Application Data

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[51] **Int. Cl.**[5] **H01L 21/265**

[52] **U.S. Cl.** **437/31**; 437/56; 437/74; 437/77

[58] **Field of Search** ..... 437/56, 57, 74, 75, 437/77, 55, 58, 59, 61, 31; 357/43, 48; 148/DIG. 9, DIG. 53, DIG. 85

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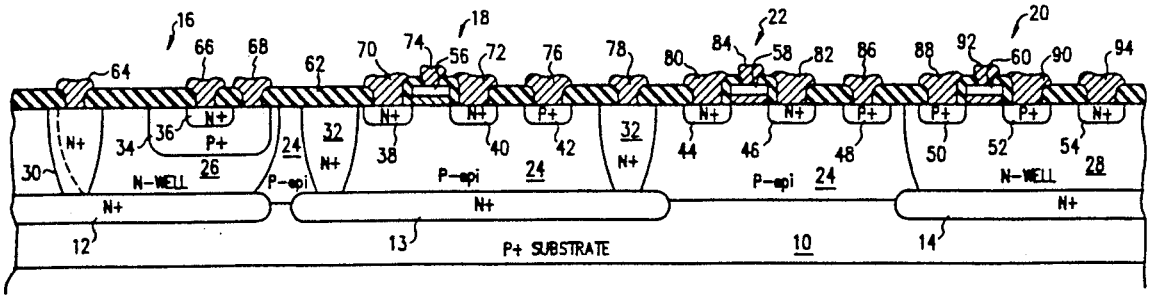
[57] **ABSTRACT**

Disclosed is a bipolar-CMOS circuit which includes a NMOS transistor site (**18**) electrically isolated from a bipolar transistor site (**16**). The NMOS transistor site (**18**) includes a semiconductor region (**24**) isolated from a bipolar transistor well (**26**) by deep diffusion ring (**32**). A buried layer (**13**) forms a bottom of the deep diffusion isolation ring (**32**). A backgate voltage can be applied to the isolated semiconductor region (**24**) of the NMOS device, which bias may be different than that applied to the substrate (**10**). Optimum performance of the NMOS transistor is thus assured irrespective of the magnitude of operating voltage of the bipolar transistor.

15 Claims, 1 Drawing Sheet