MICROSTRUCTURE FOR FORMATION OF A SILICON AND GERMANIUM ON INSULATOR SUBSTRATE OF SI1-XGEX TYPE

BACKGROUND OF THE INVENTION

The invention relates to a microstructure designed for formation of a silicon and germanium on insulator substrate of $Si_{1-Xf}Ge_{Xf}$ type, with Xf comprised between a first value that is not zero and 1, and formed by stacking of a silicon on insulator substrate and a first initial layer of silicon and germanium alloy of $Si_{1-X1}Ge_{X1}$ type, with X**1** strictly comprised between 0 and Xf.

STATE OF THE ART

The current silicon-based microelectronics technology is reaching the limits of the possibilities offered by this material. The growing need for electronic devices with better and better performances, at higher and higher speeds and with an increasingly lower power consumption has led to new solutions being studied.

The microelectronics industry then turned to germanium, which is fully compatible with the technology developed for silicon and which presents the same crystalline structure as silicon, but with better properties in terms of charge carrier mobility.

A particular application concerns pMOSFETs (p-type metal-oxide-semiconductor field-effect transistors). The article "Selectively-formed high mobility SiGe-On-Insulator pMOSFETs with Ge-rich strained surface channels using local condensation technique" by T. Tezuka et al. (2004 IEEE Symposium on VLSI Technology Digest of technical papers) in particular describes fabrication of a pMOSFET the improved performances whereof can in particular be felt for charge carrier depleted transistors (FD pMOSFET) made from germanium.

To fabricate Germanium-On-Insulator (GOI or GeOI) substrates, a first technique uses the Smart Cut™ technology, initially developed for fabrication of Silicon-On-Insulator (SOI) substrates, described in particular in the article "200 mm Germanium-On-Insulator (GeOI) structures realized from epitaxial wafers using the Smart Cut™ technology" by C. Deguet et al. (Proceedings ECS 2005, Quebec). This technology is based on transfer, onto a silicon substrate, of a germanium layer deposited on a silicon oxide layer SiO_2 forming an insulating layer. The GOI substrate obtained in this way is of the full wafer type. However, this technology presents a very high cost and nMOSFET transistors are very difficult to achieve.

A second technology is based on the lateral recrystallization principle, in particular described in the article "High-quality single-crystal Ge on insulator by liquid-phase epitaxy on Si substrates" by Y. Liu et al. (Applied Physics Letters, vol.84, n°14, Apr. 5, 2004), enabling a localized GOI substrate to be produced. The technique consists in depositing a nitride layer locally on a standard silicon substrate, which layer will form the insulator, and in then depositing a larger layer of germanium thereon, which layer will then be locally in contact with the silicon substrate. Once encapsulated, the stack is heated briefly to the melting temperature of germanium and is then cooled. Solidification of the molten germanium is initiated on the silicon of the substrate (monocrystalline seed), and the front then propagates locally forming a monocrystalline germanium on insulator layer. However, this technique for fabricating localized GOI substrates is unwieldy, due to interface stability problems, and recrystallization is limited both in extent and in geometry.

A third known fabrication technique uses the germanium condensation technique, also enabling localized GOI substrates to be obtained. This technique is based on the total miscibility of germanium and silicon (same crystalline structure) and on the difference of chemical affinities between germanium and silicon with respect to oxygen, highlighted in particular in the article "A novel Fabrication Technique of Ultrathin and Relaxed SiGe Buffer Layers with High Ge Fraction for Sub-100 nm Strained Silicon-On-Insulator MOSFETs" by T. Tezuka et al. (Jpn. J. Appl. Phys. Vol. 40 (2001) pp. 2866-2874 Part1, No. 4B, April 2001).

The article "Characterization of 7-nm-thick strained Ge-on-insulator layer fabricated by Ge-condensation technique" by S. Nakaharai et al. (Applied Physics Letters, vol. 83, n°17, Oct. 27, 2003) in particular describes the fabrication principle of a SGOI or GOI substrate by germanium condensation.

As represented schematically in FIGS. **1** and **2**, a microstructure **1** formed by stacking of a SOI substrate **2** and a layer **3** of silicon and germanium alloy of $Si_{1-X1}Ge_{X1}$ type (FIG. **1**) is designed to form a substrate **4** comprising a final layer **5** of silicon and germanium alloy of $Si_{1-Xf}Ge_{Xf}$ type (FIG. **2**).

The SOI substrate **2** of the initial microstructure **1** comprises a layer **6** of silicon oxide SiO_2 buried between two silicon layers, a thick layer **7** and a thin layer **8**, whereon the initial $Si_{1-X1}Ge_{X1}$ layer **3** is deposited. The final germanium concentration Xf in the layer **5** of the substrate **4** is comprised between a first value that is not zero and 1, and the initial germanium concentration X**1** in the layer **3** of the microstructure **1** is strictly comprised between 0 and the final germanium concentration Xf in the layer **5** of the substrate **4**.

The condensation germanium method consists in performing a thermal oxidation treatment, preferably at high temperature, of the silicon of the stack of layers of the initial microstructure **1**. As silicon has a better chemical affinity to oxygen, the germanium is not oxidized. As represented in FIG. **2**, thermal oxidation then results in consumption of the silicon of the whole of the stack of the SOI substrate **2** and of the $Si_{1-X1}Ge_{X1}$ layer **3** to form a top layer **9** of SiO_2, located on top of the substrate **4** (FIG. **2**). The thin silicon layer **8** of the SOI substrate **2**, initially arranged between the $Si_{1-X1}Ge_{X1}$ layer **3** and the buried SiO_2 layer **6** of the microstructure **1**, has been consumed during thermal oxidation and has migrated to the top layer **9** of SiO_2.

In FIG. **2**, as germanium is not soluble in SiO_2, the germanium-enriched layer **5** has been rejected against the buried SiO_2 layer **6** and then presents a smaller final thickness Ef than the initial thickness E**1** of the $Si_{1-X1}Ge_{X1}$ layer **3**.

As described in the article "Oxidation of $Si_{1-X}Ge_X$ alloys at atmospheric and elevated pressure" by D. C. Paine et al. (J. Appl. Phys. 70(9), Nov. 1, 1991), the germanium condensation process can continue until the silicon has been completely consumed so as to obtain a layer **5** containing germanium only, then forming a GOI substrate **4** with a final germanium concentration Xf equal to 1. In the case where the silicon is not completely consumed, the substrate **4** is then a SGOI substrate with a final germanium concentration Xf of the layer **5** strictly comprised between 0 and 1.

However, a major problem of this germanium condensation technique for fabrication of a substrate **4** comprising a $Si_{1-Xf}Ge_{Xf}$ layer **5** is relaxation of the strains in the germanium-enriched final layer **5**. When oxidation of the $Si_{1-X1}Ge_{X1}$ layer **3** of the microstructure **1** takes place, there is competition between silicon oxidation and germanium diffusion. A strong composition gradient can lead to a strained local state, such that the layer **5** relaxes plastically. This then results in the