HIGH VOLTAGE SEMICONDUCTOR STRUCTURE

RELATED APPLICATIONS

This is a continuation-in-part of application Ser. No. 08/966,867 filed Nov. 10, 1997.

BACKGROUND OF THE INVENTION

This invention relates to semiconductor devices and more particularly to high voltage MOSFETs.

Metal Oxide Semiconductor Field Effect Transistors ("MOSFETs") are well known and are often used in power applications because the performance characteristics of MOSFETs are generally superior to those of bipolar transistors, i.e., significantly faster switching time, simpler drive circuitry, the absence of a second-breakdown failure mechanism, the ability to be paralleled, and stable gain and response time over a wide temperature range. The major disadvantage of the MOSFET is the high on-resistance of the device.

Conventional prior art vertically conducting MOSFETs are typically fabricated using a vertical double-diffused process ("VDMOS"). The on-resistance of a VDMOS MOSFET can be generally divided into three components: (1) channel resistance, (2) neck resistance, and (3) blocking layer resistance. The channel resistance and the neck resistance of the device may be minimized during device fabrication by methods such as using finer geometries and shallower diffusions. However, the blocking layer resistance, i.e., the resistance of the layer supporting the applied voltage, is highly dependent on the breakdown voltage of the device and minimizing blocking layer resistance must be sacrificed if the device is to withstand high voltages.

FIGS. **1** and **2** show a typical prior art VDMOS MOSFET. In these devices, in order to achieve high voltage capability, the blocking layer is a thick uniformly doped layer to avoid producing high electric fields (and premature breakdown) within the device. When voltage is applied to this device, a depletion region spreads from the P-N junction downward into the uniformly doped N− blocking layer. When the integrated dopant concentration from the junction to the edge of the depletion region reaches about 1.3E12/cm2, the peak electric field at the junction is about 20 volts per micron, which is approximately the field where avalanche breakdown begins. The blocking layer of a device at breakdown contains approximately this same quantity of dopant regardless of the actual breakdown voltage. Minor variations may occur due to variations in the carrier mobility caused by factors such as temperature or dopant concentration. In the prior art device, to increase the breakdown voltage of the device, the dopant must be distributed through a greater vertical thickness causing the blocking layer to have a greater thickness as well as a higher resistivity. When breadown voltage is increased in the prior art device, the on-resistance of the device increases by a factor equal to the increase in breakdown voltage raised to the power of approximately 2.3, which is due primarily to an increase in blocking layer resistance.

Accordingly, it is an object of the present invention to provide a novel high voltage MOSFET and novel method.

It is another object of the present invention to provide a novel high voltage MOSFET with low on-resistance.

It is yet another object of the present invention to provide a novel high voltage MOSFET with low on-resistance and high breakdown voltage.

It is still another object of the present invention to provide a novel blocking layer for a high voltage MOSFET.

It is a further object of the present invention to provide a novel method of lowering the blocking layer resistance of a high voltage MOSFET while maintaining the breakdown voltage.

These and many other objects and advantages of the present invention will be readily apparent to one skilled in the art to which the invention pertains from a perusal of the claims, the appended drawings, and the following detailed description of the preferred embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a pictorial view of a typical prior art high voltage VDMOS MOSFET.

FIG. **2** is a cross-sectional view of the VDMOS MOSFET of FIG. **1**.

FIG. **3** is a pictorial view of an embodiment of a high voltage VDMOS MOSFET in accordance with the present invention.

FIG. **4** is a cross-sectional view in elevation taken through lines **4**—**4** of the VDMOS MOSFET of FIG. **3**.

FIG. **5** is a pictorial view of an embodiment of the blocking layer of the high voltage VDMOS MOSFET in accordance with the present invention.

FIG. **6** is a graphical representation of the specific resistance per breakdown voltage of the prior art MOSFET and several embodiments of the MOSFET in accordance with the present invention.

FIG. **7** is a pictorial view of another embodiment of the blocking layer of the high voltage VDMOS MOSFET in accordance with the present invention.

FIG. **8** is a pictorial view of another embodiment of a high voltage VDMOS MOSFET in accordance with the present invention.

FIG. **9** is a pictorial view of the blocking layer of the high voltage VDMOS MOSFET of FIG. **8**.

DESCRIPTION OF PREFERRED EMBODIMENTS

The embodiments illustrated herein are shown in two-dimensional views with various regions of the device illustrated as having length and width, these regions are illustrations of only a portion of the device which is comprised of a plurality of cells arranged in a three-dimensional structure.

Further, for the purposes of illustration, the preferred embodiments of the present invention are shown to include specific P and N type regions. It is understood by those skilled in the art that the teachings herein are equally applicable to a device in which the conductivities of the various regions have been reversed.

One embodiment of the VDMOS MOSFET in accordance with the present invention is shown in FIGS. **3** and **4**. With reference to FIGS. **3** and **4**, wherein like elements are given like reference numerals, the VDMOS MOSFET **10** of the present invention comprises an N+ substrate **12** with the drain contact **14** disposed on one side and a blocking layer **16** disposed on the other side. Adjacent the side of the blocking layer **16** opposite the substrate **12** are P well regions **18** and N+ source regions **20**. The N regions **22** are disposed between the P well regions **18**. A gate poly region **24** overlies the N regions **22** and the portions of the P well regions **18** and the source regions **20** adjacent the N regions