SEMICONDUCTOR DEVICES AND FABRICATION METHODS THEREOF

FIELD OF THE INVENTION

The present invention relates to semiconductor devices and methods of fabricating semiconductor devices.

BACKGROUND OF THE INVENTION

Modern integrated circuit designs may include a variety of different semiconductor device types optimized for different functions. For example, field-effect transistors are widely used to provide digital functions, such as logic, memory, or processing. Other types of semiconductor devices, such as bipolar junction transistors and rectifiers, are desirable to provide analog functions, such as temperature detection, electrostatic discharge protection, amplification, or radio frequency functions. Therefore, integrated circuits combining these different types of semiconductor devices to provide both analog and digital functions are desirable. However, different device architectures of, for example, field-effect transistors and bipolar junction transistors, typically require separate fabrication processes, leading to increased complexity and cost.

BRIEF SUMMARY

The shortcomings of the prior art are overcome, and additional advantages are provided, through the provision, in one aspect, of a semiconductor device. The semiconductor device includes: a substrate, the substrate including a p-type well adjoining an n-type well; a first p-type region and a first n-type region disposed within the n-type well of the substrate, where the first p-type region at least partially encircles the first n-type region; and a second p-type region and a second n-type region disposed in the p-type well of the substrate, where the second n-type region at least partially encircles the second p-type region.

In another aspect, a method is presented. The method includes providing a semiconductor device including a substrate, the substrate including a p-type well adjoining to an n-type well. The providing includes: fabricating a first p-type region and a first n-type region disposed within the n-type well of the substrate, and a second p-type region and a second n-type region disposed within the p-type well of the substrate, where the first p-type region at least partially encircles the first n-type region, and the second n-type region at least partially encircles the second p-type region.

Additional features and advantages are realized through the techniques of the present invention. Other embodiments and aspects of the invention are described in detail herein and are considered a part of the claimed invention.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

One or more aspects of the present invention are particularly pointed out and distinctly claimed as examples in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the invention are apparent from the following detailed description taken in conjunction with the accompanying drawings in which:

FIG. **1**A is a plan view of one embodiment of a structure including a semiconductor device, in accordance with one or more aspects of the present invention;

FIG. **1**B is a cross-sectional elevational view of the structure of

FIG. **1**A, taken along line **1**B-**1**B thereof, in accordance with one or more aspects of the present invention;

FIG. **1**C is an isometric view of another embodiment of a structure including a semiconductor device, in accordance with one or more aspects of the present invention;

FIG. **1**D is a cross-sectional elevational view of the structure of

FIG. **1**C, taken along line **1**D-**1**D thereof, in accordance with one or more aspects of the present invention;

FIG. **1**E is a plan view of one embodiment of a bipolar junction transistor, in accordance with one or more aspects of the present invention;

FIG. **1**F is a cross-sectional elevational view of the bipolar junction transistor of FIG. **1**E, taken along line **1**F-**1**F thereof, in accordance with one or more aspects of the present invention;

FIG. **1**G is a plan view of one embodiment of a bipolar junction transistor, in accordance with one or more aspects of the present invention;

FIG. **1**H is a cross-sectional elevational view of the bipolar junction transistor of FIG. **1**G, taken along line **1**H-**1**H thereof, in accordance with one or more aspects of the present invention;

FIG. **1**I is a plan view of one embodiment of a semiconductor controlled rectifier, in accordance with one or more aspects of the present invention; and

FIG. **1**J is a cross-sectional elevational view of the semiconductor controlled rectifier of FIG. **1**I, taken along line **1**J-**1**J thereof, in accordance with one or more aspects of the present invention.

DETAILED DESCRIPTION

Aspects of the present invention and certain features, advantages, and details thereof, are explained more fully below with reference to the non-limiting examples illustrated in the accompanying drawings. Descriptions of well-known materials, fabrication tools, processing techniques, etc., are omitted so as not to unnecessarily obscure the invention in detail. It should be understood, however, that the detailed description and the specific examples, while indicating aspects of the invention, are given by way of illustration only, and not by way of limitation. Various substitutions, modifications, additions, and/or arrangements, within the spirit and/or scope of the underlying inventive concepts will be apparent to those skilled in the art from this disclosure.

In one implementation, an integrated circuit design may include multiple different device types at different locations to perform different functions. During integrated circuit and semiconductor fabrication processing, millions, billions or more devices of these devices, such as transistors, capacitors, rectifiers, and resistors, may be formed to enable logic circuits, memory storage elements, or analog components. The semiconductor fabrication process is very complex, and techniques that tend to reduce complexity can improve yield and reduce costs. Cost reductions may be achieved by, for example, the elimination or consolidation of process steps, or the simplification of designs.

For example, as described herein, several advantages may be realized by defining a single universal device design that may be adapted to act as multiple different device types, leading to reduced design and maintenance costs. For instance, a universal design layout for multiple semiconductor devices may be developed to enable multiple different