

Thus, selected conditions within the processor may be used to condition the sampling of selected event(s), such as the condition of the current instruction being within the range of the S/370 PER (program-event recording) registers (IAWR), or the condition that a unique latch has been set through a state-controlling instruction (e.g. SIE or diagnose in S/370XA).

The output buffer control for event sampling is as follows:

When the ITA is full (i.e. indicated by incrementing the TAC to its highest count), inputting from gates 31 into ITA 32 is inhibited, and a signal is provided on line 33B to cause the outputting of the ITA to the associated out buffer in the PCE storage. Then TAC is reset to the first ITA address on its address bus, and the ITA is again filled, etc.

A second table address counter (not shown) may be provided in box 33 to provide the input address to the ITA, so that inputting via gates 31 may continue into half of the ITA while its other half is outputted under control of addresses generated by TAC. Thus by outputting half of the ITA at a time, the other half is concurrently available to receive event samples. The outputting of the first and second halves of ITA is controlled by a first-half full signal on line 33A and a second-half full signal on line 33B. (Alternatively, when only a single TAC is used for both input and output of the ITA, inputting to the ITA is locked out, i.e. inhibited, during its outputting to avoid potential interference.)

When the Nth signal on bus 110 reaches the ITA control gates 31, that enables the storing of an event sample in the ITA 32 at the current address indicated by TAC.

The measurement operations for an ITU during event sampling are eventually terminated according to the commands which specified the measurement.

The data flow in the CPU involves its various sub-elements that forward instrumentation data through lines 31A to 31Z as the machine signal interface to the ITU. These data signal inputs are the same for event sampling mode as they are for time sampling mode, except that for event sampling the event-related signals are forward via paths 103, 105 and 111A for the processing of selected event(s)/condition(s) into recording samples. Storing in an ITA entry can occur only at the instant when a signal is provided on bus 110, so that each sample inputted into the ITA 32 corresponds to a single occurrence of the selected event(s)/condition(s) upon each Nth occurrence.

If address generator uses only one TAC counter for both ITA input addressing and output addressing, the CPU signals received by the ITA gates 31 are stored in the ITA only if: (1) A trigger signal on bus 110 is provided from Nth event control 109, and (2) the ITA input is not locked while the TAC in the address generator 33 outputs the filled ITA content to its out buffer.

A requirement for the implementation of event sampling is that the data for recording a sample inputted to ITA 32 must convey the machine state existing at the time the pertinent machine signals were generated in the CPU. In other words, the machine state data recorded in the ITA must be reasonably contemporary with the signals representing the occurrence of the event. This requirement might fail to be met if substantial delay were to occur in the signal processing in boxes 104, 102, 107, 109 and 31, or through some kind of lookahead that tries to anticipate a future machine state.

In CPUs comprised of very high speed logic circuits, it may not be possible in a single machine cycle to operate control logic 102, 104, 107, 109 and gates 31, and still be able to record the selected data in ITA 32 in the same cycle, or even in the next cycle. In such case, a greater delay may become necessary for sampling the machine states in the ITA, for example three cycles after the occurrence of a selected event signal. In such case, the data path to the ITA may not be precisely timed with the CPU generation of the event signals.

If such substantial delay exists, the recorded sample data will to some extent not fully represent the true event environment. The degree of representation loss will depend on the amount of delay.

The PCE activity during system measurement controls the operation of the associated out buffer. The PCE monitors each out buffer and causes it to be written to disk when full. The PCE also logs a count of overruns of each ITA. Overruns indicate data loss; and depending on their frequency, overruns may affect the measurement accuracy of a run. If the user has specified an overrun threshold as a particular number of overruns, a measurement run may be terminated if the overrun threshold is reached.

Although this invention has been shown and described with respect to a single embodiment thereof, it should be understood by those skilled in the art that various changes and omissions in the form and details of the invention may be made therein without departing from the spirit and the scope of the invention.

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. Internal processor instrumentation means for monitoring the software/hardware operations of a data processing system, which includes one or more processors, a system control console having displaying screens under control of a system operator; each processor having machine cycling circuits, and I/O controls; each processor having a plurality of internal lines for transferring internal signals including signals indicating processor condition states; an event-driven monitoring means comprising:

signal collection means for registering internal signals occurring during one or more machine cycles, the signal collection means being connected to and located in proximity to internal signal lines in a processor,

condition selection logic means having inputs connected to internal lines for receiving selected internal signals indicating condition states in the processor and determining the condition states to be used in the determination of monitoring events in event-driven monitoring operations for the processor,

event selection logic means having inputs connected to the signal collection means and to the condition selection logic means, the event selection logic means determining the occurrence of a monitoring event from selected inputs from the condition selection logic means and the event selection logic means, and the event selection logic means having an output for signalling the occurrence of a monitoring event to be used in a monitoring operation, an internal instrumentation table unit (ITU) having an instrumentation table array (ITA) that includes a plurality of ITA entries and includes addressing means for selecting a current entry in the ITA, gating means being associated with the signal collection means for selecting and transmitting registered