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(54) **PROGRAMMABLE LOGIC DEVICE**

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(58) **Field of Classification Search**
CPC ..... H03K 19/17736; H03K 19/17724 (Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,352,940	A	10/1994	Watson
5,731,856	A	3/1998	Kim et al.
5,744,864	A	4/1998	Cillessen et al.
5,808,942	A	9/1998	Sharpe-Geisler
6,057,704	A	5/2000	New et al.
6,127,702	A	10/2000	Yamazaki et al.
6,150,838	A	11/2000	Wittig et al.
6,172,521	B1	1/2001	Motomura
6,208,163	B1	3/2001	Wittig et al.
6,288,569	B1	9/2001	Wittig et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	1737044	A	12/2006
EP	2226847	A	9/2010

(Continued)

OTHER PUBLICATIONS

Ishii.T et al., "A Poly-Silicon TFT With a Sub-5-nm Thick Channel for Low-Power Gain Cell Memory in Mobile Applications", IEEE Transactions on Electron Devices, Nov. 1, 2004, vol. 51, No. 11, pp. 1805-1810.

(Continued)

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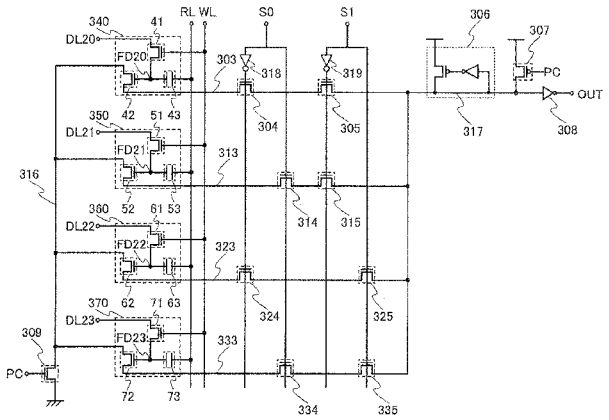
(57) **ABSTRACT**

A PLD in which a configuration memory is formed using a nonvolatile memory with a small number of transistors and in which the area of a region where the configuration memory is disposed is reduced is provided. Further, a PLD that is easily capable of dynamic reconfiguration and has a short startup time is provided. A programmable logic device including a memory element, a selector, and an output portion is provided. The memory element includes a transistor in which a channel is formed in an oxide semiconductor film, and a storage capacitor and an inverter which are connected to one of a source and a drain of the transistor. The inverter is connected to the selector. The selector is connected to the output portion.

13 Claims, 16 Drawing Sheets