advantages as listed below. These advantages are particularly remarkable in the case of thyristors using the structures according to the present invention.

(1) The turn-off time (the sum of the minor carrier storage time t_s and the fall time t_f) can be shortened and the turn-off switching energy E_{OFF} can be reduced. The reduction of the minor carrier storage time t_s, in particular, allows very easy-to-use devices which can be applicable to a high-frequency PWM inverter and so on. Besides, since the minority carrier storage time t_s can be reduced for each segment, variations in the device loss in each segment on the wafer is reduced—this allows ease in increasing diameter of the wafer.

(2) Since the main electrode shorted structure markedly decreases the quantity of gate pull-out charges and increases the tun-off gain, the gate driver can be simplified and miniaturized; thus, manufacturing costs of the semiconductor devices can be cut.

(3) The withstand voltage characteristic and the leak current under high temperature conditions are about the same as in the prior art and the steady loss is low at the time of steady blocking. Hence, while the turn-off performance is enhanced, it is possible to keep excellent the on-state characteristic which usually has a trade-off relation to the turn-off performance.

(4) Since the on-state voltage V_T has a positive temperature characteristic, thermal runaway is not likely to occur during high-frequency operation, in particular; therefore, the devices of the present invention can be used at high frequencies.

(5) Even if the turn-off speed is raised extremely high, equal to that of the SI transistor, for example, substantially no influence is exerted on the firing. That is, it is substantially unchanged with the waveforms of the gate voltage and the gate current at turn-on switching. Even if the turn-off performance is enhanced, the turn-on switching loss E_{ON} undergoes substantially no change in the low current region. In the high current region the turn-on rise time t_r and the turn-on switching loss E_{ON} tend to increase, but the delay time t_d does not change. It is also possible to produce an effect of increasing the surge capability in the high current region.

Needless to say, SI transistors utilizing the structures according to the present invention could also benefit from the effects (1) through (5) referred to above with respect to thyristors.

It will be apparent that many modifications and variations may be effected without departing from the scope of the novel concepts of the present invention.

What is claimed is:

1. A static induction semiconductor device with a distributed main electrode structure, which has a first main electrode region formed in a first main surface of a high resistivity layer, a second main electrode region formed in the first or second main surface of said high resistivity layer, and a control region formed near said first main electrode region and in which said control region forms a channel region in said high resistivity layer and controls the height of a potential barrier in said channel region to control a main current between said first main electrode region and said second main electrode region, characterized in that said first main electrode region has a structure wherein regions of higher and lower impurity densities relative to each other are distributed and that a main electrode formed in contact with said first main electrode region is partly in contact with said lower impurity density region as well as said higher impurity density region, and said higher and lower impurity density regions in said first main electrode region are the same in conductivity type but opposite to said control region.

2. The static induction semiconductor device of claim **1**, characterized in that said main electrode formed in contact with said first main electrode region makes ohmic contact with said higher impurity density region and non-ohmic or Schottky contact with said lower impurity density region.

3. The static induction semiconductor device of claim **1**, characterized in that said main electrode in contact with said first main electrode region is formed of aluminum (Al), molybdenum (Mo), tungsten (W), platinum (Pt), titanium (Ti), nickel (Ni) or their silicon (Si)-base alloys or silicides.

4. The static induction semiconductor device of claim **1**, characterized in that said higher impurity density region in said first main electrode region is composed of separated regions.

5. The static induction semiconductor device of claim **1**, characterized in that said control region has a buried structure.

6. The static induction semiconductor device of claim **1**, characterized in that said control region has a recessed structure.

7. The static induction semiconductor device of claim **1**, characterized in that said control region has a planar structure.

8. The static induction semiconductor device of claim **1** is a static induction thyristor.

9. The static induction semiconductor device of claim **1** is a static induction transistor.

10. A static induction semiconductor device with a static induction main electrode shorted structure, which has a first main electrode region formed in a first main surface of a high resistivity layer, a second main electrode region formed in said first or second main surface of said high resistivity layer, and a control region formed near said first main electrode region and which said control region forms a channel region in said high resistivity layer and controls the height of a potential barrier in said channel region to control a main current between said first main electrode region and said second main electrode region, characterized in that said first main electrode region has a structure wherein regions of higher and lower impurity densities relative to each other and a short-circuit region respectively formed in said lower impurity density region surrounded by said higher impurity density regions are distributed, that a main electrode formed in contact with said first main electrode region is partly in contact with said lower impurity density region and said short-circuit region as well as said higher impurity density region, that said short-circuit region is of the same conductivity type as said control region but is opposite to said higher impurity density region and that a potential barrier is formed in said lower impurity region between said short-circuit region and said control region by a depletion layer spreading from said higher impurity density region into said lower impurity density region, and said higher and lower impurity density regions are of the same conductivity type but opposite to said control region.

11. The static induction semiconductor device of claim **10**, characterized in that said main electrode formed in contact with said first main electrode structure makes ohmic contact with said higher impurity density region and non-ohmic or Schottky contact with said lower impurity density region.