11. The semiconductor structure of claim **10**, further comprising a conductive plug between the active portion of the metal structure and the first semiconductor die.

12. The semiconductor structure of claim **10**, wherein the dummy bump is configured to connect with a dummy pattern external to the three dimensional stack.

13. The semiconductor structure of claim **10**, further comprising a PPI on the first semiconductor die and electrically coupled to the first semiconductor die.

14. The semiconductor structure of claim **1**, wherein the metal structure further comprises a redistribution layer (RDL) connecting to the passive surface of the semiconductor die.

15. The semiconductor structure of claim **1**, further comprising a dummy bump connected to the dummy portion of the metal structure, wherein the dummy bump comprises a three dimensional surface.

16. The semiconductor structure of Claim **3**, wherein the passive surface of the semiconductor die is contacting a bottom of a recess of the RDL.

17. The semiconductor structure of claim **6**, wherein the PPI is electrically connected to the active surface of the semiconductor die.

18. The semiconductor structure of claim **12**, wherein the dummy pattern is electrically connected to a redistribution layer (RDL).

19. The semiconductor structure of claim **18**, wherein a recess portion of the RDL is contacting the backside of the second semiconductor die.

20. The semiconductor structure of claim **10**, further comprising a PPI on the first semiconductor die and electrically coupled to the active portion of the metal structure.

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