

DIGITALLY SYNTHESIZED AUDIO FREQUENCY VOLTAGE SOURCE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention pertains to voltage waveform generation systems and more particularly to the digital generation of synthetic alternating current voltage waveforms in the audio frequency range.

2. Related Prior Art

Digitally-synthesized sine-wave sources have become commonplace in metrology laboratories in recent years, particularly where a precise knowledge of the phase angle between two waveforms is required. Impedance and power bridges, as well as phase angle rely on waveform synthesis techniques to achieve state-of-the-art accuracy. The approach has been applied to ac-voltage with some success; however, imperfections in the steps used to generate the waveforms have limited the ability to calculate the rms value of the ac signal based on a knowledge of the static voltage of each step. Transient energy due to waveform aberrations at the step transitions (often referred to as "glitches") adds to the signal power making it difficult to predict the rms value accurately.

SUMMARY OF THE INVENTION

The present invention provides a method and apparatus for accurately generating a digitally synthesized sinusoidal voltage which is started by storing digital values for sine waveforms in a read only memory. A first digital to analog converter is connected to the read only memory through a first latch. A second digital to analog converter is connected to the read only memory through a second latch. The output of the first digital to analog converter and the output of the second digital to analog converter is alternatively switched between the inverting input and the non-inverting input common of an operational amplifier such that the first digital to analog converter is connected to the inverting input while the second is connected to the non-inverting input. The output of the operational amplifier is connected to the inverting input through a variable capacitance, the feedback being determined by the digital to analog converter connected to the inverting input. A clock is used to control the connection of the first and second digital to analog converter to the inverting input and to control the determination of the feedback.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic block diagram of a digitally synthesized voltage source.

FIG. 2 is a graphical representation of a sine wave approximation generated using a single digital to analog converter.

FIG. 3 is a graphical representation of a sine wave approximation using the digitally synthesized source of FIG. 1.

FIGS. 4-7 are graphical representations of the results of step and thermal measurements of the digitally synthesized voltage source of FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A "deglitching" technique has been employed to enhance the step quality in an audio-frequency, digitally synthesized source (DSS). Charge-coupled and switch-

ing glitches, as well as current settling time in high-resolution digital-to-analog converters (DAC), may be reduced by toggling between two converters which are updated at different times.

A simplified diagram of the digitally synthesized source 12 of the present invention is shown in FIG. 1. Digital values of the waveform, stored in a read-only-memory (ROM) 14 are latched sequentially by latches 16 and 18 into multiplying digital to analog converters, MDAC 20 and MDAC 22, on the positive transition of clock signals A and B, respectively. Fast CMOS switches 24, 26, 28 and 30 steer the output current from each MDAC to ground 32 until the current step has settled, and then steer the current into the inverting input 34 of a wide band operational amplifier 36. At time t_1 new data is latched by latch 16 into MDAC 20, switches 26 and 28 are closed, and switches 24 and 30 are opened. While MDAC 20 is settling, MDAC 22 supplies the output step, and thus most of the transient energy generated by MDAC 20 is dissipated in the ground plane. At time t_2 , new data is latched via latch 18 into MDAC 22, switches 24 and 30 are closed, and switches 26 and 28 are opened. MDAC 20 now supplies the output step while MDAC 22 is settling. Each MDAC 20 and 22 supplies half of the steps and thus operates at half of the clock rate, allowing the generator to operate at higher clock rates than would be possible with a single digital to analog converter.

The feedback path, from the amplifier output back to its inverting input, is determined by either MDAC 20 or 22, whichever is connected to the inverting input. In addition to the gain accuracy and temperature tracking realized by using the internal feedback resistor in each MDAC, this approach minimizes the effects of switch contact-resistance (inside the feedback loop the switch resistance is divided by the amplifier loop gain).

An oscilloscope trace of a portion of a one hundred twenty-eight step sine-wave approximation generated by a single digital to analog converter with a clock rate of 1 MHz is shown in FIG. 2. The corresponding waveform, generated by toggling two digital to analog converters, such as the present invention, into the same output stage, is shown in FIG. 3. The major transition glitch Z and glitch Y, as well as other structural differences between the steps in the single digital to analog converter system are virtually eliminated with the two digital to analog converter approach.

While the waveform in FIG. 3 is noticeably improved, the flatness of its rms (root mean squared) value vs. frequency is not well defined (at the ppm level) above about 2 kHz. The deglitching technique does not eliminate the effects of charge injection from the logic signals into the switches, timing skews in the switches and in the control signals, or amplifier errors (including overshoot, ringing, and slew limiting). In the frequency band from 2 to 15 kHz these effects tend to increase the rms value as the frequency is increased. By sacrificing frequency response, the amplifier can be band limited to flatten the rms gain to within ± 10 ppm, well into the audio-frequency range. This trimming is done using a small variable capacitor 38, which shunts the feedback circuit of the output amplifier.

In the preferred embodiment of the present invention, digitally synthesized source 12 has been constructed using eighteen bit multiplying digital to analog converters as MDAC 20 and 22. For simplicity only the most-significant eight bits are used to synthesize the wave-