

provide considerable benefit to accurate and timely demodulation of received signals and the extraction of data therefrom, particularly for bursty, brief data packets. As contrasted with the known prior art in which various of the portions of circuits similar to the circuits of the baseband processor of FIG. 3 have been provided by separate hardware devices and/or by separate complex programmable devices, the present invention is particularly suited to integration into a single device.

The baseband processor of FIG. 3 may be used to transfer packetized data received in the form of serial data in a physical layer to a media access control ("MAC") layer imbedded in the packetized data are header information used to control the physical layer. The header information may include fields of preamble/sync, unique word, signal field, service field, length field and a CRC field. The signal field is used to specify the signalling type used to modulate the data: either DPSK or QPSK. In one embodiment, the processor may receive data in which the header is in BPSK but the data is in QPSK. In such situations, the timing of switching the receiver from one signalling format to another is time critical. In another aspect of the present invention, the number of fields in the header may be user selectable.

It is known in the prior art that interfaces between the physical layer and the MAC level may be either serial or parallel. Most prior art implementations are parallel because the of the severe timing restrictions in which parallel circuits permit quicker timing but at the considerable additional expense of parallel hardware. Often the physical layer tasks of header generation and detection are done at the MAC layer, usually by separate devices. In contrast, in the present invention, all of the header detection and similar physical layer tasks may be imbedded into a single device.

In prior art devices where the header and similar physical layer tasks are handled by separate circuits/devices, there passes some period of time between when the circuit detects and demodulates an acceptable header and the transmission of that state to the circuit demodulating the data. In the present invention, where the number of bits in the header is held to a minimum and may be used to determine which of plural antennae are to be used in addition to the other customary header functions, the slip of a single bit may mean the difference between successfully decoding a message and missing the message.

During demodulation of the header, the present invention monitors and uses the header data to both identify the type of signalling to be used for the data but to select between plural antennae. By using the data developed in the preamble for immediate data decoding, the number of lost bits is minimized. In receiving the header, the baseband processor converts the serial data from the data descrambler 104 into a 16 bit parallel word which is compared with the preselected values for the unique word and the signalling fields. The unique word is searched for a fixed amount of time and if it is not found, the modulator/demodulator is reset and acquisition of the RF signal is restarted. Once the unique word is found, a field counter searches through the incoming bits in a parallel fashion for the fields making up the header. As each field is detected, the received data is stored into internal registers for access through the serial control bus the signalling field, when detected, is used to switch the receiver modulator/demodulator between BPSK and QPSK at the correct time with respect to the data portion of the packet. When the length field is detected, this value is loaded into a counter and is used to track the incoming bits of the data packet and to signal the MAC layer when the last bit of the packet is received. The processor interface 114 may also

compute the CRC on the fly and compare the computed CRC to the CRC received within the message. If the CRCs do not match the receive data packet may be terminated and the receiver reset into reacquisition.

While preferred embodiments of the present invention have been described, it is to be understood that the embodiments described are illustrative only and the scope of the invention is to be defined solely by the appended claims when accorded a full range of equivalence, many variations and modifications naturally occurring to those of skill in the art from a perusal hereof.

What is claimed is:

1. A circuit for detecting a message header in a signal which has been transmitted using direct sequence spread spectrum modulation, comprising a single device having:

means for receiving an analog signal having modulated thereon in a spread spectrum format a message having a header portion and a data portion;

means for converting said analog signal into a digital signal;

means for demodulating the header of the digital signal using digital binary phase shift keyed (BPSK) demodulation and for demodulating the data portion of the same message using quaternary phase shift keyed demodulation (QPSK);

means contained on said single device for timing a transition from BPSK modulation to QPSK modulation; and,

means for providing the demodulated data signal to a media access control (MAC) layer.

2. The circuit of claim 1 further comprising means for adjusting said means for timing to account for headers of variable length.

3. The circuit of claim 2 wherein said means for adjusting is contained within said single device and wherein said means for adjusting is responsive to a data field within said message header.

4. The circuit of claim 1 wherein said single device is a single monolithic device.

5. The circuit of claim 1 wherein said analog signal is in the form of in-phase and quadrature components.

6. The circuit of claim 5 wherein the data within said signal is modulated using PN modulation and phase shift keyed modulation.

7. The circuit of claim 5 further comprising means to evaluate during the header portion of the message the signals received from plural antennae and to select one of said antennae for use during the receipt of the data portion of the same message.

8. The circuit of claim 7 wherein the circuit is contained on a single monolithic device.

9. The circuit of claim 8 wherein said circuit acquires a unique word within a message header and if no unique word is acquired within a predetermined period of time resets the circuit.

10. In a communication system capable of receiving RF direct sequence spread spectrum signals, said system having a message header detection circuit comprising a single device having:

an analog receiver for receiving a spread spectrum modulated signal having a header portion and a data portion; an analog-to-digital converter operable on said modulated signal;

a digital demodulator for binary phase shift keyed (BPSK) demodulation of said header portion and quaternary phase shift keyed (QPSK) demodulation of said data portion;