

variety of conditions through a level adjust circuit 82. The A/D converters may be three bit converters which each provide their digital outputs to correlator circuits 84, 86 which acquire the signal of interest by detecting the pseudorandom noise ("PN") code in use for the particular spread spectrum link. The correlators 84, 86 may be matched filter correlators which (1) despread the wideband direct sequence spread spectrum ("DSSS") signal information to convert it back to the original data rate; and (2) spread unwanted interfering signals and noise to separate them spectrally from the data.

The correlators 84, 86 may receive a PN code of variable length, programmable up to 16 bits. The correlators 84, 86 are each dedicated to one of the component channels (I and Q) and have a common correlation reference which can be varied in both length and sequence to permit the system to be used to demodulate a wide variety of signal types. As is explained in more detail in the copending application entitled "SHORT BURST ACQUISITION CIRCUIT FOR DIRECT SEQUENCE SPREAD SPECTRUM LINES" filed on even date herewith, and incorporated herein by reference, the received signal may be sampled at twice the chip rate and the correlators have taps on every other stage. The output signal from the correlators are converted from I and Q form to polar form by a cartesian to polar converter 88. The polar form of the signal is used in the remainder of the demodulator processing, reducing the need for duplicate hardware for the independent I and Q channels.

A symbol tracking and timing circuit 90 is used to track the peak correlation magnitude and to control chip timing resolution to plus/minus one-quarter chip. The symbol tracking and timing circuit 90 can be a circuit such as described in more detail in "FAST ACQUISITION BIT TIMING LOOP METHOD AND APPARATUS", filed on even date herewith and incorporated herein by reference. The symbol tracking and timing circuit 90 averages the individual correlator samples over a desired period, such as the dwell period of the system on one of the antennae during the preamble. By averaging the samples, the effect of noise is reduced, permitting an improved ability to resolve a small early or late bias.

In the tracking and timing circuit 90, the magnitude of the correlator output amplitudes are accumulated modulo the number of samples in a symbol. In this way, a sum of the correlator magnitudes is formed at each one sample phase of symbol timing. The best sample phase will produce a discernible peak with smaller samples on either side. All other samples will generally consist of accumulated noise and will be smaller in the sum of magnitudes. If the received signal is strong, the magnitudes provided by the correlator will be large and, in conventional designs, would have required an accumulator and other downstream equipment to maintain extra bits to prevent overflow. In contrast, in the present invention, overflow is prevented in large signals while maintaining accuracy on poor signals by barrel shifting the accumulations of magnitude when the largest value gets above one-half full scale. In one embodiment of the present invention, this value can be readily trapped by tracking the most significant bit ("MSB") of the accumulation. When the MSB of an accumulation is set to 1 (all numbers from the correlator are magnitudes and therefore positive), all of the accumulations and the subsequent outputs of the correlator are right shifted by one bit. The number of shifts may be counted and is similar in fashion to an exponent. Thus, the sample having the largest sum of magnitudes may be identified without adding extra bits to the accumulators and downstream equipment while maintaining, with the accu-

mulator and exponent, and absolute indication of the strength of the received signal.

With continued reference to FIG. 3, the polar signal produced by the cartesian to polar converter 88 is provided to a PSK demodulator 100, and in turn to a differential decoder 102 and to a data descrambler 104. The PSK demodulator can demodulate both BPSK and QPSK signaling. In one aspect of the present invention, the preamble of a received signal may be in BPSK format and the data of the received signal may be in either BPSK or QPSK format. Because QPSK and BPSK signals are modulated differentially, the symbol information is based upon the state of the previous symbol. Phase errors introduced by multipath and oscillator offset drifts are compensated by a phase locked carrier tracking loop 108. In one embodiment, the loop uses an NCO providing eight bits of phase output to the PSK demodulator 100, and may be variously set to track and adjust for phase offset errors by rotation of the signal phase. The phase and frequency information developed during the preamble of a message is used to preset the loop 100 for minimum loop settling time.

With continued reference to FIG. 3, in one embodiment of the present invention, signal quality (SQ) and signal frequency (SF) measurements are made simultaneously with symbol timing measurements. When the bit synch level, signal quality (SG) and the Received Signal Strength Indicator (RSSI) are all above their respective thresholds, the received signal is declared present. As explained in detail in co-pending U.S. application Ser. No. 509,586, entitled "A METHOD OF ESTIMATING SIGNAL QUANTITY FOR A DIRECT SEQUENCE SPREAD SPECTRUM RECEIVER", filed on even date herewith and incorporated herein by reference, decisions as to which of two antennae would be used to receive data can be made after taking measurements during the dwell period for each antenna. Once a particular antenna is selected, the measured symbol timing and carrier frequency offset for the selected antenna is jammed into the symbol timing and into the phase-locked-loop of the NCO tracking the carrier to begin carrier de-rotation. In this way, the demodulating circuitry gets a "head start" in reacquiring and demodulating the incoming preamble data within the brief period desired for bursty communications.

The data descrambler 104 may be a self synchronizing circuit having programmable (or user settable) taps comprising 7 bit shift registers. For data to be transmitted, a similar data scrambler 110 is used. The data scrambler 110 can be selectively disabled for measuring RF carrier suppression, during which an alternating 1/0 pattern is transmitted. Likewise, the data descrambler may be selectively disabled to permit data to pass without change from the differential decoder 102 to the processor interface 114.

Data to be transmitted may be received from an external device by the processor interface 114. The processor interface 114 may generate a preamble, CRC and other protocols to be sent along with the data and to provide the data and other protocol signals to the data scrambler 110 and to a differential encoder 116 to develop PN modulated I and Q signals which can be provided to a quadrature IF modulator such as the modulator 42 of FIG. 2 for eventual transmission on an antenna.

Descrambled data may be provided to a processor interface 114 which may control the passage of the data to another device such as a media access control ("MAC") circuit.

With continued reference to FIG. 3, it has been found that placing the entire baseband processor onto a single chip can