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a timer for transitioning between the BPSK demodulation and the QPSK demodulation; and,

an interface for providing the demodulated data signal to a media access control (MAC) layer.

11. The circuit of claim 10 wherein said timer is adjustable to account for headers of variable length. 5

12. The circuit of claim 11 wherein the adjustability of said timer is based on information contained within a data field of said header portion.

13. The circuit of claim 10 further comprising antenna selection circuitry for selecting, upon evaluation of said header portion obtained from a plurality of antennae, one of said plurality for receipt of the associated data portion of said header portion. 10

14. The circuit of claim 13 wherein the circuit is contained on a single monolithic device. 15

15. The circuit of claim 14 wherein said circuit acquires a unique word within said header portion and if no unique word is acquired within a predetermined period of time the circuit resets. 20

16. The circuit of claim 10 wherein the analog signal received is in the form of in-phase and quadrature components and the data within the signal is modulated using PN modulation and phase shift keyed modulation.

17. A direct sequence spread spectrum receiver, said receiver having a physical layer associated with the receiv- 25

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ing of RF signals and a media access control (MAC) layer associated with the using of data within said RF signals, said physical layer comprising a single device having:

an analog receiver for receiving a spread spectrum modulated signal having a header portion and a data portion; an analog-to-digital converter operable on said modulated signal;

a digital demodulator for binary phase shift keyed (BPSK) demodulation of said header portion and quaternary phase shift keyed (QPSK) demodulation of said data portion;

a timer for transitioning between the BPSK demodulation and the QPSK demodulation; and,

an interface for providing the demodulated data signal to said MAC layer.

18. The receiver of claim 17 wherein the single device transmits the data from said physical layer to said MAC layer in a serial data stream.

19. The receiver of claim 18 wherein the single device is a single monolithic device.

20. The receiver of claim 17 wherein the data is modulated within the signals by both PN and phase shift keyed modulation.

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