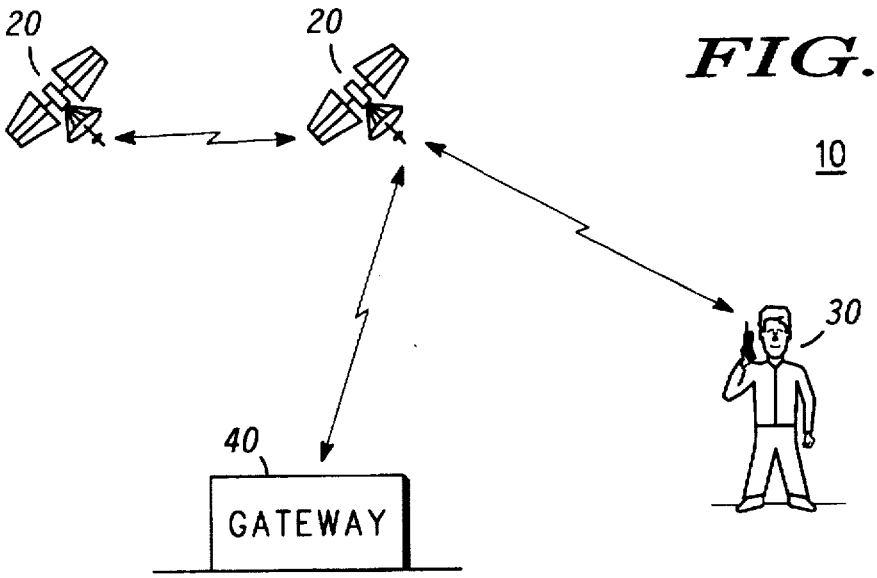
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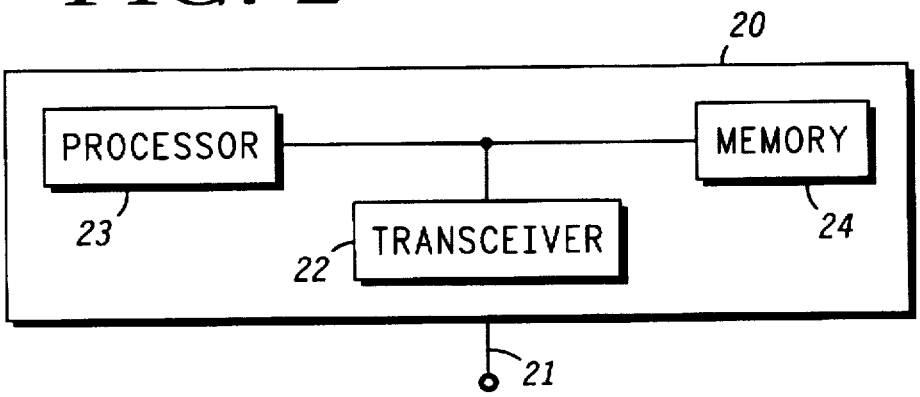
GATEWAY

FIG. 1

FIG. 2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PROCESSOR
MEMORY
23
TRANSCEIVER
22
24
21