

For example, the top-gate TFT structure can be a low temperature polycrystalline silicon (LTPS) TFT structure.

According to another aspect of the present invention, there is provided a process for manufacturing a thin film transistor (TFT) planar display panel. The process includes steps of providing a light-transmissible substrate, forming a light-shielding structure on the light-transmissible substrate, and forming a first buffer layer and a top-gate TFT structure on the resulting substrate in sequence with a channel region of the top-gate TFT structure substantially aligned with the light-shielding structure.

Preferably, the light-shielding structure is formed by sputtering a light-shielding layer on the light-transmissible substrate, and defining and etching the light-shielding layer by a photolithographic process.

Preferably, the process further includes a step of forming a second buffering layer on the light-transmissible substrate prior to the formation of the light-shielding structure so as to dispose the light-shielding structure between the first and second buffering layers.

Preferably, the top-gate TFT structure is produced by steps of successively forming a semiconductor layer and a photoresist on the first buffer layer on a first side of the light-transmissible substrate, providing an exposing source opposite to the first side with the light-shielding structure as a mask to define an exposed portion and a non-exposed portion of the photoresist, and then removing the exposed portion of the photoresist, using the unexposed portion of the photoresist as a mask to proceed a heavily doping ion implantation procedure on the semiconductor layer to form source/drain regions, successively forming a gate insulating layer and a first conductive layer on the semiconductor layer, and then performing a first masking and photolithographic procedure on the first conductive layer to form a gate conductive structure of the top-gate TFT structure, forming a dielectric layer on the gate insulating layer formed thereon the gate conductive structure, and then performing a second masking and photolithographic procedure on the gate insulating layer and the dielectric layer to form a contact hole, and forming a second conductive layer on the dielectric layer in connection with the source/drain regions through the contact hole, and performing a third masking and photolithographic procedure on the second conductive layer to form a source/drain connecting line structure.

Preferably, the top-gate TFT structure further includes lightly doped drain regions that are formed by using the gate conductive structure as a mask to proceed a lightly doping ion implantation procedure on the semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may best be understood through the following description with reference to the accompanying drawings, in which:

FIG. 1 is a schematic circuit diagram illustrating a pixel unit of a conventional thin film transistor liquid crystal display (TFT-LCD);

FIGS. 2A–2C are schematic cross-sectional diagrams illustrating the steps of a conventional process for producing a low temperature poly silicon thin film transistor (LTPS-TFT) of a TFT-LCD;

FIGS. 3A–3G are schematic cross-sectional diagrams illustrating a preferred embodiment of a process for producing a TFT-LCD panel according to the present invention; and

FIGS. 4A–4F are schematic cross-sectional diagrams illustrating another preferred embodiment of a process for producing a TFT-LCD panel according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention will now be described more specifically with reference to the following embodiments. It is to be noted that the following descriptions of preferred embodiments of this invention are presented herein for purpose of illustration and description only; it is not intended to be exhaustive or to be limited to the precise form disclosed.

The present invention provides a TFT-LCD panel structure and a process for producing the TFT-LCD panel structure for solving the current-leakage problem resulting from the illumination of the back light source on the channel region. The TFT-LCD panel structure according to the present invention includes a light-shielding structure formed between the back light source and the top-gate TFT structure, and substantially aligned with the channel region for protecting the channel region from the illumination of the back light source. Thus, the current leakage problem of the devices occurring when the TFT is OFF will be efficiently reduced.

Please refer to FIGS. 3A–3G which are schematic cross-sectional diagrams illustrating the steps of a process for producing a TFT-LCD panel according to the present invention. First of all, as shown in FIG. 3A, a light-shielding layer 30 is formed on a light-transmissible substrate 300. Then, a light-shielding structure 301 is defined and etched by a masking and photolithographic process, as shown in FIG. 3B. Please now refer to FIG. 3C. A buffer layer 302 and an amorphous silicon (a-Si:H) layer 31 are successively formed on the resulting light-transmissible substrate 300 with the light-shielding layer 301. Then, the amorphous silicon layer 31 is converted into a polysilicon layer 304 by a laser crystallizing process. Please refer to FIG. 3D. A photoresist layer is formed on the polysilicon layer 304, and exposed by a back light source with the light-shielding structure 301 as a mask. The exposed portion of the photoresist is removed. The non-exposed portion of the photoresist forms a photoresist mask structure 305 as shown in FIG. 3D. Then, a heavily doping ion implantation procedure proceeds to form source/drain regions 306 in the polysilicon layer 304 by using the structure 305 as a mask, as shown in FIG. 3E. After removing the photoresist mask structure 305, a gate insulating layer 307 and a conductive layer are formed on the resulting structure in sequence, and the conductive layer is further defined and etched by a masking and photolithographic process to form a gate conductive structure 308 as shown in FIG. 3F. Then, lightly doped drain regions 309 are formed by a trace N-type dopant implantation procedure with the gate conductive structure 308 as a mask. Please refer to FIG. 3G. After an interlayer dielectric layer 310 is formed on the resulting structure of FIG. 3F, a further masking and photolithographic process is performed to define contact holes 32 at proper positions. Then, another conductive layer is formed on the interlayer dielectric layer 310 and fills with the contact holes 32, and is defined and etched to form a source/drain connecting line structure 311 by a masking and photolithographic process. Thus, a top-gate TFT structure including a channel region 312 is formed on the buffer layer 302 with the light-shielding structure 301 substantially aligned with the channel region 312 to protect the channel region 312 from illumination of the back light source.