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[54] **METHOD OF MAKING MOS TRANSISTORS WITH A GATE-SIDE AIR-GAP STRUCTURE AND AN EXTENSION ULTRA-SHALLOW S/D JUNCTION**

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[52] **U.S. Cl.** **438/305**; 438/595; 438/657

[58] **Field of Search** 438/305, 306, 438/307, 595, 657

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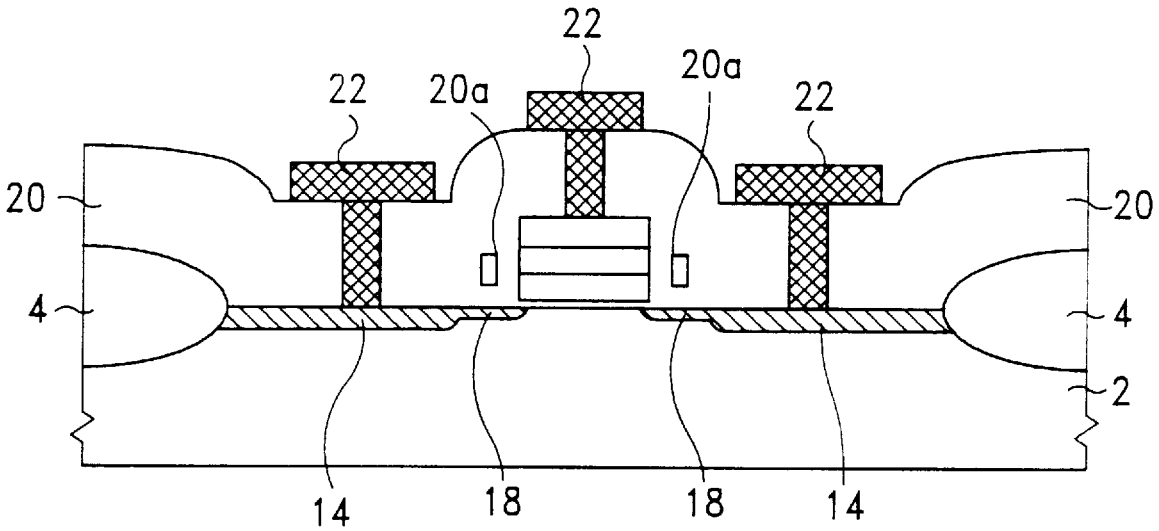
[57] **ABSTRACT**

This invention proposes a new process to form MOS transistor with a gate-side air-gap structure and an extension ultra-shallow S/D junction for high speed devices. After growing the thin gate oxide film on silicon substrate, a stacked-amorphous-Si (SAA) film is deposited. A thin CVD oxide film is deposited and then patterned. The top two amorphous-Si layers are etched back and then form the nitride spacers. The pad CVD oxide film is removed by diluted HF solution followed by S/D/G implant. High temperature thermal oxidation process is used to convert the bottom amorphous-Si layers outside the nitride spacers into thermal oxide and simultaneously to form shallow junction. The nitride spacers are removed and then the low energy/high dose ion implantation is performed for extension S/D junction. The bottom amorphous-Si layer is etched back and then RTP anneal in N_2O or NO ambient is used to recover the etching damage to form an extension S/D junction. A thick CVD oxide film is deposited on all regions. Due to the step coverage issue, a air-gap structure would be formed at the gate side.

22 Claims, 4 Drawing Sheets