transistor structure. The platinum silicide **170** resides within the gate and the oxide layer **108***b* is therefore located under the gate.

At step **206**, the extra platinum layers **160** located along the side walls of the trench are removed using a selective etch, e.g., using a hydrogen peroxide or "SC1" process. It is appreciated that the selective etching step does not remove the silicide layer **170**. Next, the extra second spacer material **128'** located along the side walls of the trenches is removed using a diluted HF solution. Lastly, the extra polysilicon **124** along the sides of the trench walls is removed using a diluted solution of NH_4 and HF (NH_4HF), or any other well known chemical process may also be used. The net result of the above steps **200** is shown in FIG. **18**. The only remaining chemicals in the sides of the trench walls are the first spacer **112**/**114** which may optionally be removed.

At step **208**, the trenches are filled with oxide **108***c* and then etched back (trench etch) using well known processes. Contact etching is then performed. A metal is used as the contacts, e.g., aluminum may be used.

The result of the fabrication process **200** is shown in FIG. **19** which illustrates a MESFET structure **250** in accordance with an embodiment of the present invention. The gate is formed sideways. In this embodiment, the drain in located at the bottom and the source is located at the top. The oxide layer **108***b* under the gate is instrumental in reducing gate to drain capacitance. Also, the small surface of the p-n junction acts to reduce its capacitance. In other words, the exposure of the p-n junction is reduced in order to substantially reduce the junction capacitance over the prior art designs. The gate region silicide layer **170** is useful in reducing the gate resistance. The very thin gate, e.g., 1000 angstroms or less, results in fast switching speed, therefore, the MESFET structure **150** is good in high frequency applications. It is appreciated that the narrow gate also yields a small RDS on (on resistance, drain to source). Also, the protruding p regions **140** reduce the junction capacitance of the device.

The formation of the windows **120** (FIG. **8**) provides great control for the formation of the gate in the amount of diffusion that is performed based on the amount of oxide that dipped off during the fabrication of the MESFET **250**. This allows Vt to be tightly controlled based on the window size.

As a result of the above features, and specially due to the oxide layer **108***b* below the gate, the novel MESFET structure **250**, which can be used in a normally-on or normally-off mode, has: (1) reduced gate current; (2) reduced gain-drain capacitance; and (3) low gate resistance.

Because the MESFET **250** can be used in a mode of operation that is forward bias through the gate, the smaller p-n junction at the gate is effective to reduce otherwise wasted current flow there through. Another advantage of the MESFET structure **250** is that it is fabricated in a vertical orientation with respect to the substrate. Therefore, the structure **250** can be made more compact and therefore may be densely packed for dense IC designs.

The preferred embodiment of the present invention, transistor structures (JFET and MESFET) for low voltage, high current and high frequency applications, are thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

What is claimed is:

1. A MESFET structure comprising:
an n+ type substrate forming a drain;
an n type substrate disposed on said n+ type substrate and comprising a trench etched therein;
an n+ type layer disposed on said n type substrate and forming a source thereon;
an oxide bottom layer disposed in a well of said trench;
a silicide layer disposed on said oxide bottom layer and forming a gate and extending laterally into said n-type substrate;
an oxide fill layer disposed within said trench and on said silicide layer; and
metal contacts.

2. A MESFET structure as described in claim **1** wherein said silicide layer is platinum silicide.

3. A MESFET structure as described in claim **2** wherein said silicide layer is approximately 1000 angstroms in height within said trench.

4. A MESFET structure as described in claim **1** wherein said oxide bottom layer is approximately 2000 angstroms in height.

5. A MESFET structure as described in claim **1** wherein said oxide bottom layer is for reducing gate to drain capacitance.

6. A MESFET structure as described in claim **1** wherein said silicide layer is for reducing gate resistance.

7. A MESFET structure as described in claim **1** wherein said MESFET is a normally off MESFET device.

8. A transistor structure comprising:
an n+ type substrate forming a drain;
an n type substrate disposed on said n+ type substrate and comprising trenches etched therein;
an n+ type layer disposed on said n type substrate and forming a source thereon;
oxide bottom layers disposed in wells of said trenches;
silicide layers disposed on each oxide bottom layer and forming a gate;
p type regions disposed within said n-type substrate and adjacent to edges of said silicide layers creating p-n junctions between said trenches, wherein each p type region includes a first p type sub-region disposed within said n-type substrate and a second p type sub-region disposed on each oxide bottom layer; and
oxide fill layers disposed within each trench and on said silicide layers.

9. A transistor structure as described in claim **8** wherein said silicide layer is platinum silicide and wherein said transistor is a MESFET transistor.

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