to produce a single, discrete HVFET on a die of virtually any (within practical limits) rectilinear-shape.

FIG. **8** illustrates an example gate metal routing layout for the die shown in FIG. **7**. The gate metal routing scheme of FIG. **8** is fabricated using a single metal layer process with both source and gate metal disposed on the same planar level. The example shown includes horizontal gate metal bus lines **41***a*-**41***d* that run between each row of the checkerboarded blocks of racetrack-shaped HVFET segments. For example, gate metal bus lines **41***a* & **41***b* are shown extending horizontally along the top and bottom of the first (upper) row of checkerboarded sections **36** of FIG. **7**. (It is appreciated that gate metal bus line **41***b* may be twice as wide as bus line **41***a* due to the face that bus line **41***b* provides a shared conduction path to the polysilicon gate members of both the first and second rows of checkerboarded sections.)

Within each row, the sections **36** that have the length of their transistor segments aligned in the x-direction have half of the polysilicon gate members coupled to the top bus line, and a second half of the polysilicon gate members coupled to the bottom bus line. For instance, the upper left-hand block or section **36** in FIG. **8** is shown having the polysilicon gate members represented by lines **44***a* connected to gate metal bus line **41***b* via contacts **45***a*, whereas the polysilicon gate members represented by lines **44***b* in the same section are connected to gate metal bus line **41***a* via contacts **45***b*. Note that each line **44***a* or **44***b* actually represents the two gate members **18***a* & **18***b* (see FIG. **1**) of a single racetrack-shaped HVFET segment. Thus, lines **44***a* represent the gate members of the two left-most HVFET segments, and lines **44***b* represent the gate members of the two right-most HVFET segments, in the same section. Note further that each gate member is connected to a bus line (top or bottom) at one end only.

The gate metal routing pattern shown in FIG. **8** also includes vertical gate metal stub lines **42** that extend approximately half-way across each row of checkerboarded blocks. Within each section in which the length of the HVFET segments is aligned in the y-direction, half of the polysilicon gate members are coupled to one stub line, and the other half of the polysilicon gate members are coupled to another stub line. For example, the second section (from the left) in the upper row of FIG. **8** shows a bottom half of the gate members (represented by lines **44***c*) connected to left-sided gate metal stub line **42***a* via contacts **45***c*, with a top half of the gate members (represented by lines **44***d*) connected to right-sided gate metal stub line **42***b* via contacts **45***d*. Similarly, the fourth section (right-hand most) in the upper row of FIG. **8** shows a bottom half of the gate members connected to gate metal stub line **42***c* and a top half of the gate members connected to gate metal stub line **42***d*. Note that each gate member of the horizontally-aligned segments is connected to a stub line (left or right side) at one end only.

The reason why gate metal stub lines **42** extend only half-way across those sections having their segments aligned in the y-direction (i.e., horizontally) is to allow the source metal bus lines to extend across each row and contact the source regions of each transistor segment. This is illustrated by the example of FIG. **9**, which shows a die **25** having individual source bus lines **61** that extend continuously across each row of transistor sections **36** between top and bottom gate metal traces **51**. (Metal traces **51** represent the merged metal bus lines **41** and stub lines **42** associated with each row.) For example, source bus lines **61***a* runs continuously across the upper row of sections on die **25** to contact each of the source regions **14** at the top of silicon pillars **17** for each HVFET segment in the row. In so doing, source bus lines **61***a* "snakes" between and around stub lines **42**, as well as between bus lines **41**, all of which are patterned on the same single layer of metal.

Practitioners in the art will appreciate that by extending stub lines **42** approximately half-way across each row, the current handling capability of each source bus line **61** is maximized (i.e., minimum notching of lines **61**). To put it differently, extending stub lines **42** vertically (in the x-direction) a distance other than half-way across each row would unnecessarily constrain or pinch current flow across source bus lines **61** due to the notching of lines **61** around stub lines **42**. Likewise, it should be understood that by connecting half of the gate members in a section to one gate metal bus (or stub) line, and the other half to another gate metal bus (or stub) line, electro-migration and resistance problems are minimized.

FIG. **10** illustrates an expanded portion of the example layout shown in FIG. **9** that shows one possible scheme for connecting gate metal trace **51** with gate members **18***a* & **18***b*. In this example, via contacts **55***a* & **55***b* are shown connecting trace **51** with the rounded fingertip portion of gate members **18***a* & **18***b*, respectively. The source region at the top of pillar **17** located between gate members **18***a* & **18***b* is shown connected to source metal bus **61** via contacts **75**. (It is appreciated that only two contacts **75** are shown for clarity reasons.) In an alternative embodiment, rather than contacting the rounded fingertip portion of gate members, gate metal trace **51** may connect along the straight, linear portion of gate members **18***a* & **18***b* near the rounded fingertip portion. (Note that the field plates are not shown in the example of FIG. **10** for clarity reasons.)

Although the above embodiments have been described in conjunction with a specific device types, those of ordinary skill in the arts will appreciate that numerous modifications and alterations are well within the scope of the present invention. For instance, although HVFETs have been described, the methods, layouts and structures shown are equally applicable to other structures and device types, including Schottky, diode, IGBT and bipolar structures. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

I claim:

1. A transistor comprising:

a plurality of transistor segments organized into a plurality of sections, each transistor segment having a length and a width, the transistor segments of each section being arranged in a side-by-side relationship along the width, the sections being arranged in rows and columns, the sections of each row being arranged such that section-to-section the length of the transistor segments is alternately aligned in first and second lateral directions, the first lateral direction being substantially orthogonal to the second lateral direction, each transistor segment including:

a pillar of a semiconductor material, the pillar having a source region disposed at or near a top surface;

first and second dielectric regions disposed on opposite sides of the pillar, respectively;

first and second gate members respectively disposed in the first and second dielectric regions; and

a first metal layer that includes a source bus coupled to the source region of each transistor segment, and a gate bus coupled to the first and second gate members of each transistor segment.

2. The transistor of claim **1** wherein the pillar extends in the first and second lateral directions to form a racetrack-shaped ring or oval.