

Referring to FIG. 9, a block diagram of a circuit 100' is shown illustrating a five phase SCSI driver. The circuit 100' may be similar to the circuit 100. The circuit 100' may comprise a number of current sources 106a-106n and 108a-108n and a number of flip-flops 150a-150n and 152a-152n. A number of current sources 106a-106n, current sources 108a-108n, flip-flops 150a-150n and flip-flops 152a-152n may be varied in order to meet the criteria of a particular implementation. The current sources 106a-106n and 108a-108n may be weighted to influence pulse shapes of the differential waveform. The switches A, B, C and D may also be weighted. In one example, the circuit 100 may implement the individual current sources 106a-106n and 108a-108n and the equally weighted switches A, B, C, and D to control current switching. The circuit 100' may also implement a number of clock phases (e.g., CL1, CL2, CL3, CL4 and CL5).

The current sources 106a-106n may be implemented as P-channel current sources. The switches A and B may be implemented as P-channel switches. The current sources 108a-108n may be implemented as N-channel current sources. The switches C and D may be implemented as N-channel switches. In one example, each of the current sources 106a-106n and 108a-108n may be implemented as a 2 mA current source. However, the particular size of the current sources 106a-106n and 108a-108n may be varied accordingly to meet the design criteria of a particular implementation. Additionally, the current source 106a and the current source 108a may act as offset cancellation current sources.

In one example, five switches with equal weighting and combined current sources are typically implemented for SCSI Ultra3. SCSI Ultra3 I/O devices may control rise time with a 3:1 variation across PVT. In another example, five switches with binary (e.g., 1,2,4,2,1) weighting may be implemented for SCSI Ultra4. SCSI Ultra4 may implement binary switch weighting to open the eye (to be discussed in connection with FIGS. 7 and 8). SCSI Ultra4 may also use a current controlled delay line for generation of multiphase data. The current controlled delay line may provide 1.5:1 variation across PVT. Such an implementation may improve operation of conventional SCSI Ultra4 devices.

Referring to FIG. 10, a circuit 200' is shown. The circuit 200' may be similar to the circuit 200. The circuit 200' may be configured to generate the clock phases CL1-CL5. The circuit 200' may generate the clock phases CL1-CL5 in response to the signal DATA. The clock generation circuit 200' may trigger on data transitions of the signal DATA.

Conventional LVD transmitters in multi-drop cable environments require edge-rate control to avoid generation of crosstalk and reflection noise. However, such conventional solutions are configured to slow down the output data at the output (or last) stage for a timed transition at the output. The circuit 100 may be configured to separate the timing for LVD edge-rate control out of the critical data path. Specifically, the timing circuit 200 may not be implemented in the critical data path. Therefore, the timing circuit 200 may not delay the output differential waveform of the circuit 100. The circuit 100 may detect when the output on the pins V+ and V- is about to change state and trigger the timing circuit 200 to control the transmitted edge rate.

The circuit 100 may implement the parallel drivers 180a and 180b to improve transmitter ISI precompensation. The circuit 100 may also implement the parallel weighted current sources 106a-106n and 108a-108n to improve ISI precompensation. The circuit 100 may implement weighted switching to improve the transition levels in the current-mode

driver 100 (or 190). The overall impedance of the switches A, B, C and D may be set by a predetermined common-mode range requirement. The individual impedance of each switch A, B, C, and D may be optimized, such that when turning on the total resistance of all switches N, at a particular point changes by 1/N. The circuit 100 may therefore avoid a case when first and last switch are small compared to the termination resistance.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. An apparatus comprising:

a first plurality of parallel switches configured to (i) each receive a multiphased data signal having N phases, where N is a positive integer and (ii) control a voltage on a first output pin; and

a second plurality of parallel switches configured to (i) each receive a digital complement of said multiphased data signal and (ii) control a voltage on a second output pin, wherein said first and second pluralities of parallel switches are configured to provide rise time control of a differential waveform.

2. The apparatus according to claim 1, wherein a timing between a first and a last phase of said multiphased data signal is configured to determine a rise and fall time of said differential waveform.

3. The apparatus according to claim 1, wherein each of said first and second pluralities of parallel switches are weighted to determine a pulse shape of said differential waveform.

4. The apparatus according to claim 1, further comprising: one or more current sources configured to provide current to each of said first and second pluralities of parallel switches.

5. The apparatus according to claim 4, wherein said one or more current sources comprises parallel current sources.

6. The apparatus according to claim 5, wherein each of said parallel current sources are weighted to determine a pulse shape of said differential waveform.

7. The apparatus according to claim 1, further comprising: a first driver configured in parallel; and

a second driver configured in parallel, wherein said first and second drivers are configured to synchronize to a phased clock signal.

8. The apparatus according to claim 7, wherein said first and second drivers are configured to perform pre-emphasis on said differential waveform.

9. The apparatus according to claim 8, wherein said first and second drivers are configured to mitigate effects of intersymbol interference (ISI).

10. The apparatus according to claim 7, wherein said first driver comprises a main driver and said second driver comprises a secondary driver.

11. The apparatus according to claim 7, wherein said first driver comprises one or more flip-flops and said second driver comprises one or more flip-flops.

12. The apparatus according to claim 7, wherein said first and second drivers are clocked by a multiphase clock signal.

13. The apparatus according to claim 12, further comprising:

a clock generation circuit configured to generate said multiphase clock in response to a data signal and a precompensation signal.