

14. The apparatus according to claim 1, wherein a first phase and a second phase of a multiphase clock signal are configured to set a rise and fall time for said differential waveform.

15. The apparatus according to claim 14, wherein generation of said first phase and said second phase are controlled by a bias.

16. The apparatus according to claim 1, wherein said apparatus is configured to overcome cable induced effects.

17. The apparatus according to claim 1, wherein said apparatus is further configured to synchronize a plurality of drivers to provide precompensation.

18. The apparatus according to claim 1, wherein said positive integer N, is three or more.

19. An apparatus comprising:

means for controlling a voltage on a first output pin with a first plurality of parallel switches each receiving a multiphased data signal having N phases, where N is a positive integer;

means for controlling a voltage on a second output pin with a second plurality of parallel switches each receiving a digital complement of said multiphased data signal; and

means for providing rise time control of a differential waveform, wherein said first and second pluralities of parallel switches are driven by a phased data signal.

20. A method for implementing small computer systems interface (SCSI) equalization, comprising the steps of:

(A) controlling a voltage on a first output pin with a first plurality of parallel switches each receiving a mul-

tiphased data signal having N phases, where N is a positive integer;

(B) controlling a voltage on a second output pin with a second plurality of parallel switches each receiving a digital complement of said multiphased data signal; and

(C) providing rise time control of a differential waveform, wherein said first and second pluralities of parallel switches are driven by a phased data signal.

21. An apparatus comprising:

a first plurality of parallel switches configured to control a voltage on a first output pin;

a second plurality of parallel switches configured to control a voltage on a second output pin, wherein said first and second pluralities of parallel switches are configured to provide rise time control of a differential waveform and are driven by a phased data signal;

a first driver and a second driver configured in parallel, wherein said first and second drivers (i) are configured to synchronize to a phased clock signal and (ii) are clocked by a multiphase clock signal; and

a clock generation circuit configured to generate said multiphase clock in response to a data signal and a precompensation signal, wherein a first phase and a second phase of said multiphase clock signal are configured to set a rise and fall time for said differential waveform.

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