CIRCUIT AND METHOD FOR DRIVING A JUNCTION FIELD EFFECT TRANSISTOR

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims benefit to U.S. Provisional Patent Application Ser. No. 60/792,295, filed Apr. 14, 2006, entitled "Circuit and Method for Driving a Junction Field Effect Transistor," which is incorporated herein by reference in its entirety.

This application also related to U.S. Pat. No. 6,661,276, which issued on Dec. 9, 2003, entitled "MOSFET Driver Matching Circuit for an Enhancement Mode JFET," which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

The present invention relates to the field of field effect transistors (FETs). More specifically, embodiments of the present invention relate to circuits and methods for driving a junction field effect transistor.

BACKGROUND

Field Effect Transistors (FET) include metal oxide semiconductor FET (MOSFET) devices and junction FET (JFET) devices. Historically, the use of MOSFETs has been more widespread than that of JFETs. As a result of their widespread use, driver circuits and other circuits for MOSFETs are readily and economically available. One such circuit is a MOSFET based converter circuit.

A schematic of a typical MOSFET converter circuit **100** is shown in Prior Art FIG. **1**. MOSFET converter circuit **100** includes a driver circuit **110**, which functions as a gate driver. MOSFET gate driver **110** is configured to drive high side MOSFET Q**102** and low side Q**1** MOSFET Q**101**. Driver **110** generates high peak currents for switching the MOSFETs Q**101** and Q**102** on and off.

Resistors R**111** and R**112** are typically relatively small value resistors. Resistors R**111** and R**112** deter oscillations. The high side gate switching waveform V**2** is in phase with the driver input signal V**1**. The low side gate switching waveform V**3** is out of phase with input signal V**1**. A high output from driver U**110** turns on the MOSFETs Q**102** and Q**101**.

Converter circuit **103** has an output inductor L**131** and output filter capacitor C**141**. The inductive-capacitive network of converter **103** convert the switching waveform of Q**101** and Q**102** to a DC output voltage Vo.

Although significant bias current is not needed at the gates of MOSFETs Q**102** and Q**101**, in applying their full bias voltage, power is dissipated in resistors R**111** and R**112**. This dissipation of power reduces the efficiency of driver circuit **100**.

Junction field effect transistors (JFETs) are majority carrier devices that conduct current through a channel that is controlled by the application of a bias voltage to a p-n junction. Minimal on state drain-source resistance (R_{DSOn}) characterizes efficient device performance. Low R_{DSOn} is typically achieved with a significant DC driving current I_{Bias} providing the voltage to bias the FET.

Although MOSFET based circuitry is readily and economically available, a growing demand for JFET based circuitry has developed. In part, this is understandable from advances that have accompanied the adoption of submicron processes for device fabrication, such as operationally higher speeds and lower voltages. For instance, greater current demands in integrated circuits have resulted in JFET based circuitry, such as in power conditioning. Exemplary circuits include buck converters and switching power supplies.

Switching mode regulators are preferred to linear devices due to considerations related to efficiency. For instance, efficiency can be increased by operating a switch (e.g., the transistor) so that it is either fully on or fully off. Circuits used to drive a transistor for a switching application are designed with the goal of providing a fast transition between the "on" and "off" states of the transistor switch.

JFETs are capable of being driven by low voltages while maintaining excellent breakdown characteristics when compared to MOSFETs. There is no insulator associated with gate/drain and gate/source interfaces of a JFET (e.g., these interfaces comprise p-n junctions). Thus, forward bias results in conduction at voltages that are very low compared to the reverse bias that the device is capable of withstanding. JFETs also have a much greater resistance to damage from electrostatic discharge (ESD) than MOSFETs. Thus, JFET circuit use may be preferable to MOSFET circuits for a particular application.

Due to the fundamental differences between MOSFETs and JFETs, conventional MOSFET drivers such as circuit **100** are not well suited for driving JFETs. For instance, while MOSFETs may be biased without significant bias current I_{Bias}, modern JFET bias currents range from 1 to 200 mA.

One approach to providing sufficient JFET biasing current has been to provide a direct drive from a gate driver circuit. The voltage of such drivers can range in some applications from 5 to 12 V. A schematic of a conventional JFET direct drive gate driver circuit **200** is depicted in prior art FIG. **2**. Direct JFET driver circuit **200** supplies high peak switching currents as well as the DC bias current in the range of 1 ma to 200 ma.

Circuit **200** directly drives JFET transistors Q**203** and Q**204** in that the DC bias current is supplied from the voltage driver U**210** itself. Circuit **200** also provides negative voltage to the gates when the JFETs Q**203** and Q**204** are in an "off" state. This negative voltage keeps the JFET in a low leakage off state, which supports proper operation for depletion JFETs.

Capacitors C**222** and C**223** in the gate circuits **224** and **225**, respectively, provide the high peak switching drive currents. Resistors **8233** and R**234** set the DC gate bias currents. The negative voltage is generated because the positive voltage at the gate is clamped by a gate to source diode effect within each JFET when the driver voltage goes positive. MOSFETs, such as Q**101** and Q**102** (FIG. **1**) do not have this built in diode effect between gate and source.

The high side gate switching waveform V**4** is in phase with the driver input signal V**1**. The low side gate switching waveform V**5** is out of phase with input signal V**1**. When the driver voltage swings to 0V, the voltage at the JFET gate swings to a negative voltage because it was clamped at +0.7V when the driver output voltage was high.

Converter circuit **203** has an output inductor L**231** and output filter capacitor C**241**. The inductive-capacitive network of converter **203** converts the switching waveform of Q**203** and Q**204** to a DC output voltage Vo.

Circuit **200** functions to drive the JFETs Q**203** and Q**204**. However, driving I_{Bias} directly can consume significant power, which can adversely affect the efficiency of the power supply. For instance, in applying full bias voltage to JFETs Q**203** and Q**204**, the bias currents may dissipate significant power in resistors R**233** and R**234**, which thus typically have relatively high wattage ratings.