Reference is now made to FIG. **6** which illustrates a structure **50** including the substrate shown in FIG. **1**E and at least one MOS, particularly a pMOS **52**, located on a surface of the Si film **18'**; at least one nMOS (not shown) can be formed in an active area of the substrate to the periphery of the active area illustrated in this drawing. Although the pMOS is shown on the substrate provided in the first embodiment of the present invention, the pMOS can be formed on any of the substrates described and illustrated in the second-fifth embodiments of the invention. The pMOS **52** includes an optional interfacial layer **54**, a high k gate dielectric **56** located either on a surface of the optional interfacial layer, if present, or atop the SiGe film **25** (e.g., the combination of Si cap **21** and the oxidized and stripped SiGe film **18'**) if the interfacial layer is not present, and a gate conductor **58** atop the high k gate dielectric **56**. At least one optional spacer **60** made by present on the sidewalls of at least the gate conductor. The structure also includes source/drain diffusion regions **62** at the footprint of the patterned gate region.

The at least one pMOS **52** shown in FIG. **6** is fabricated utilizing conventional processing techniques well known to those skilled in the art. For example, the at least one pFET **52** can be formed by any sequence of deposition, lithography, and etching. One typical method to form the pMOS is to first form the optional interfacial layer utilizing a conventional growth technique (such as, for example, a wet chemical oxidation). Next, a stack containing the gate dielectric and gate electrode is formed by deposition, and thereafter lithography and etching is used to form a patterned gate region. The optional spacer **60** may then be formed by deposition and etching, followed by ion implantation and annealing, which steps are used to form the source and drain diffusion regions **62**. Alternatively, a replacement gate process using a dummy gate can be used. So as not to obscure the invention, the details concerning the processing of the pMOS structure **52** are not provided herein.

The various elements of the pMOS **52** are now described in greater detail. With respect to the interfacial layer **54**, the interfacial layer **54** is comprised of a semiconductor oxide, semiconductor nitride, semiconductor oxynitride or a nitrided semiconductor oxide. Preferably, the interfacial layer **54** is comprised of a silicon oxide or silicon nitride. The thickness of the interfacial layer **54** is typically from 0.5 nm to 1.5 nm, with a thickness from 0.8 nm to 1.0 nm being more typical. The thickness, however, may be different depending on the processing conditions used during the formation of the layer and subsequent formation of the other elements of the PFET device.

The high k gate dielectric **56** is comprised of an insulating material having a dielectric constant of greater than SiO_2. That is, the high k gate dielectric **56** employed in the invention is any insulating material having a dielectric constant of greater than 4.0, preferably greater than 7.0. The dielectric constants mentioned herein are relative to a vacuum, unless otherwise stated. Specifically, the high k gate dielectric **56** employed in the present invention includes, but is not limited to an oxide, nitride, oxynitride and/or silicates including metal silicates, aluminates, titanates and nitrides. In one embodiment, it is preferred that the gate dielectric **56** is comprised of an oxide such as, for example, HfO_2, ZrO_2, Al_2O_3, TiO_2, La_2O_3, $SrTiO_3$, $LaAlO_3$, Y_2O_3 and mixtures thereof.

The physical thickness of the high k gate dielectric **56** may vary, but typically, the gate dielectric has a thickness from 0.5 nm to 10 nm, with a thickness from 0.5 nm to 2 nm being more typical.

The optional at least one spacer **60** is typically comprised of an insulating oxide, nitride, and/or oxynitride as well. The width of the optional at least one spacer **60**, as measured at the bottom of the spacer, may vary, with typical ranges being from 20 nm to 80 nm. The gate conductor **58** is comprised of any conductive material including, for example, polysilicon, SiGe, an elemental metal, an alloy including an elemental metal, a metal silicide, a metal nitride or any combination thereof including multilayers. The thickness of the gate conductor **58** may vary, with typical thicknesses being from 20 nm to 200 nm.

It is observed that the above described elements represent basic elements that are present in most pMOS devices. Although description and illustration is shown for the above pMOS elements, the present invention also contemplates other MOS elements including raised source/drain regions, silicide regions, BEOL interconnect structures, etc. It is also observed that an nMOS may also be formed atop the SiGe film provided in the present invention, however a greater benefit is observed when the pMOS is formed thereon since the substrate is engineered to alter the bandgap of the substrate favorably for a pMOS.

While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

What is claimed is:

1. A structure including a SiGe engineered channel comprising:

a semiconductor substrate having at least one active area with an exposed upper surface comprising a semiconductor material of said semiconductor substrate, wherein isolation regions are present in said semiconductor material and are located at a periphery of said at least one active device region, each isolation region having an upper surface that is coplanar with the exposed upper surface of the semiconductor material; and

a SiGe film located directly on the exposed upper surface of the semiconductor material active area, said SiGe film including a lower region that has a first Ge concentration and an upper region that has a second Ge concentration, wherein the first Ge concentration is greater than the second Ge concentration, and wherein said SiGe film has sidewall surfaces located above the isolation regions, wherein each sidewall surface of said SiGe film is oriented perpendicular to a topmost surface of the semiconductor substrate and is vertically aligned to a sidewall edge of each isolation region that is located at the periphery of the at least one active device region.

2. The structure of claim **1** wherein said semiconductor substrate is a Si-containing semiconductor material.

3. The structure of claim **1** wherein said SiGe film includes a Si cap located atop an oxidized SiGe layer, said oxidized SiGe layer has a lower region and an upper region, wherein said lower region has a Ge concentration that is greater than 25 atomic percent and said upper region has a Ge concentration that is about 35 atomic percent or greater.

4. The structure of claim **3** wherein said Ge concentration in the lower region of said oxidized SiGe layer is about 30 atomic percent or greater and said Ge concentration in the upper region of said oxidized SiGe layer is about 35 atomic percent or greater.

5. The structure of claim **1** wherein said SiGe film is a graded SiGe layer.