US007177353B2

(12) **United States Patent**
Abnous et al.

(10) **Patent No.: US 7,177,353 B2**
(45) **Date of Patent: Feb. 13, 2007**

(54) **ARCHITECTURE FOR VERY HIGH-SPEED DECISION FEEDBACK SEQUENCE ESTIMATION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 776 days.

(21) Appl. No.: **09/804,082**

(22) Filed: **Mar. 12, 2001**

(65) **Prior Publication Data**

US 2002/0122480 A1 Sep. 5, 2002

(51) **Int. Cl.**
H03H 7/30 (2006.01)
H03H 7/40 (2006.01)
H03K 5/159 (2006.01)

(52) **U.S. Cl.** **375/233**; 375/262; 375/341

(58) **Field of Classification Search** 375/229–233, 375/262, 341; 714/792, 794, 795
See application file for complete search history.

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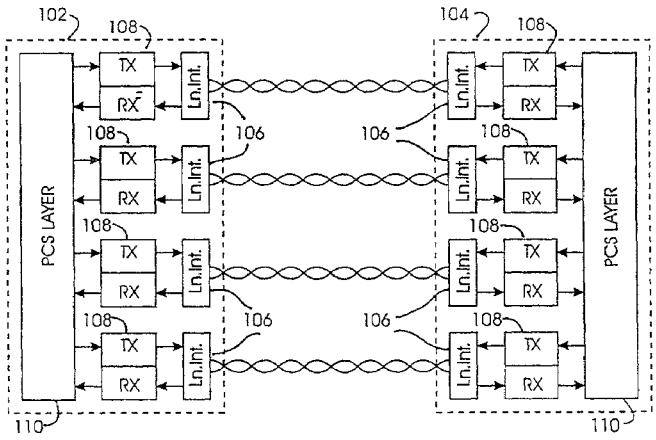
(57) **ABSTRACT**

A method for providing a next-cycle input sample from a decision feedback equalizer to a symbol decoder using look-ahead computations such that timing contention between the decision feedback equalizer and the symbol decoder is reduced. During a symbol period, a set of possible values is computed in the decision feedback equalizer and a set of path memory symbols is computed in the symbol decoder, the set of path memory symbols being based on a current input sample. During the same symbol period, one of the possible values is selected as the next-cycle input sample based on at least one of the next-cycle path memory symbols produced from the symbol decoder.

9 Claims, 22 Drawing Sheets