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[54] **CMOS OUTPUT BUFFER WITH ENHANCED ESD RESISTANCE**

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[57] ABSTRACT

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The present invention provides a CMOS integrated circuit in which core transistors are provided with punch-through pockets, while the input/output transistors are not provided with punch-through pockets. Punch-through protection for the input/output transistors by virtue of their larger dimensions. The pockets, like lightly doped drains, are formed after the gates are formed but before the formation of gate sidewalls. However, the input/output are masked during the punch-through implants, but are unmasked for at least one of the lightly doped drain implants. The absence of pockets on the input/output transistors enhances their ESD resistance, and thus the ESD resistance of the incorporating integrated circuit.

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[52] U.S. Cl. **257/357; 257/345; 257/369; 257/392**

[58] Field of Search **257/369, 357, 257/392, 345**

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5 Claims, 8 Drawing Sheets

