The invention claimed is:

1. A decryption device for decrypting encrypted signals, comprising:
an electronic circuit on a substrate having a first side;
semiconductor structures on the first side;
a copy-protect layer fixedly joined to at least a region of the semiconductor structures; and
a decryption device.

2. The electronic component with copy protection, comprising:
an electronic circuit on a substrate having a first side, said electronic circuit comprising a decryption device;
semiconductor structures on the first side; and
a copy-protect layer fixedly joined to at least a region of the semiconductor structures, wherein the copy-protect layer comprises an at least binary system of glass, and wherein the at least binary system of glass is a material that represents a synthesis of at least two chemical compounds.

3. The electronic component as claimed in claim 2, wherein the copy-protect layer comprises a first material, the first material being selected so that an etching process that dissolves the copy-protect layer destroys a portion of the electronic circuit.

4. The electronic component as claimed in claim 2, wherein the copy-protect layer is a continuous layer.

5. The electronic component as claimed in claim 2, wherein the copy-protect layer comprises a borosilicate glass with aluminum oxide and alkali metal oxide fractions.

6. The electronic component as claimed in claim 2, wherein the copy-protect layer is an evaporation coating.

7. The electronic component as claimed in claim 2, wherein the copy-protect layer shields electromagnetic waves.

8. The electronic component as claimed in claim 2, wherein the copy-protect layer is a thermal evaporation coating or an electron-beam evaporation coating.

9. The electronic component as claimed in claim 2, wherein the copy-protect layer is from 0.01 μm to 1000 μm thick.

10. The electronic component as claimed in claim 2, further comprising connection structures and elevated connection structures arranged on a second side of the substrate, the second side being on the opposite side from the first side, wherein the elevated connection structures are electrically connected to the connection structures.

11. The electronic component as claimed in claim 2, further comprising connection structures and elevated connection contacts arranged on the first side of the substrate, the elevated connection contacts being electrically connected to the connection structures.

12. The electronic component as claimed in claim 2, wherein the copy-protect layer has a first portion and a second portion that have different etching rates.

13. The electronic component as claimed in claim 3, wherein the substrate comprises a semiconductor layer of silicon and the copy-protect layer comprises silicon.

14. The electronic component as claimed in claim 10, wherein the second side is coated with plastic between the elevated connection structures so that the elevated connection structures remain uncovered.

15. The electronic component as claimed in claim 10, wherein the second side is coated with glass between the elevated connection structures so that the elevated connection structures remain uncovered.

16. The electronic component as claimed in claim 11, wherein the copy-protect layer on the first side of the substrate extends between the elevated connection contacts and the connection structures so that the elevated connection contacts and the connection structures remain uncovered.

17. A process for producing copy protection for an electronic circuit, comprising the steps of:
providing a substrate having semiconductor structures on at least a first side of the substrate;
providing a material for coating the substrate; and
coating the substrate with a copy-protect layer by evaporation coating, wherein the copy-protect layer comprises an at least binary system of glass, and wherein the at least binary system of glass is a material that represents a synthesis of at least two chemical compounds, the semiconductor structures comprising electronic decryption devices.

18. The process as claimed in claim 17, wherein the semiconductor structures, at least in regions, are covered by the copy-protect layer, the copy-protect layer being matched to the substrate so that an etching process that dissolves the copy-protect layer likewise attacks the substrate so that the semiconductor structures are at least partially destroyed.

19. The process as claimed in claim 17, wherein the copy-protect layer is a continuous layer.

20. The process as claimed in claim 17, wherein the copy-protect layer comprises a borosilicate glass with aluminum oxide and alkali metal oxide fractions.

21. The process as claimed in claim 17, wherein the copy-protect layer comprises a shield against electromagnetic waves.

22. The process as claimed in claim 17, wherein coating the substrate with the copy-protect layer comprises evaporation coating induced by thermal evaporation or by electron beam evaporation.

23. The process as claimed in claim 17, wherein the copy-protect layer is applied to the substrate in a thickness of from 0.01 to 1000 μm.

24. The process as claimed in claim 17, wherein coating the substrate with the copy-protect layer comprises coating at a bias temperature of below 300° C.

25. The process as claimed in claim 17, wherein coating the substrate with the copy-protect layer comprises coating at a pressure of from 10^{-3} mbar to 10^{-7} mbar.

26. The process as claimed in claim 17, further comprising applying a glass layer to a second side of the substrate, wherein the second side is on the opposite side from the first side.

27. The process as claimed in claim 17, further comprising applying a plastics layer to a second side of the substrate, wherein the second side is on the opposite side from the first side.

28. The process as claimed in claim 17, further comprising:
thinning the substrate;
producing etching pits with connection structure regions on the first side of the substrate;
applying a plastics layer to a second side of the substrate, wherein the second side is on the opposite side from the first side, the plastics layer being applied so that the connection structure regions remain open;
producing contacts on the second side by coating with a conductive layer;
applying a ball grid array; and
dicing the substrate into individual chips.

29. The process as claimed in claim 17, further comprising:
evaporation coating a second side of the substrate with a glass layer that is from 0.01 μm to 50 μm thick; and
uncovering connection structure regions located beneath the glass layer by grinding or etching.