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15. The quantum processor of claim 14 wherein the superconducting flux-based shift register includes a single flux quantum (SFQ) shift register.

16. The quantum processor of claim 1 wherein the memory administration system includes a routing system.

17. The quantum processor of claim 16 wherein the routing system includes a demultiplexer circuit.

18. The quantum processor of claim 1 wherein at least one DAC is configured to administer at least one analog signal to at least one programmable device.

19. The quantum processor of claim 18 wherein the at least one DAC is configured to administer the at least one analog signals to the at least one programmable device via inductive coupling.

20. The quantum processor of claim 19 wherein the inductive coupling between the at least one DAC and the at least one programmable device is mediated by an intermediate coupling device.

21. The quantum processor of claim 20 wherein at least one intermediate coupling device is configured to inductively couple to both the at least one DAC and the at least one programmable device.

22. The quantum processor of claim 21 wherein the at least one intermediate coupling device is configured to communicate to an activation communication conduit and the at least one intermediate coupling device is capable of being switched between an active state and an inactive state via the activation communication conduit.

23. The quantum processor of claim 22 wherein at least two intermediate coupling devices are configured to communicably couple to the same activation communication conduit and each intermediate coupling device is capable of being switched between an active state and an inactive state by the activation communication conduit.

24. The quantum processor of claim 22 wherein the activation communication conduit is analog variable between the active state and the inactive state.

25. The quantum processor of claim 1 wherein at least two DACs are each configured to administer at least one respective analog signal to the same programmable device.

26. A method of programming a quantum processor, wherein the quantum processor includes a plurality of programmable devices and a memory administration system having at least one digital-to-analog converter (DAC), the method comprising:

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using the memory administration system to program a first DAC with a first digital signal that embodies a control parameter for a first programmable device;

using the first DAC to convert the first digital signal to a first analog signal; and

administering the first analog signal to the first programmable device.

27. The method of claim 26 wherein using the first DAC to convert the first digital signal to a first analog signal includes generating a first analog signal having a magnitude proportional to the first digital signal.

28. The method of claim 27 wherein administering the first analog signal to the first programmable device includes administering the first analog signal to an intermediate coupling device.

29. The method of claim 28 wherein the intermediate coupling device is configurable to an active state and an inactive state and wherein the intermediate coupling device administers the first analog signal to the first programmable device when the intermediate coupling device is in the active state.

30. The method of claim 28 wherein the intermediate coupling device is tunable between an active state and an inactive state and wherein the intermediate coupling device administers at least a portion of the first analog signal to the first programmable device when the intermediate coupling device is tuned away from the inactive state.

31. The method of claim 26, further comprising: using the memory administration system to program a second DAC with a second digital signal that embodies a control parameter for a second programmable device; using the second DAC to convert the second digital signal to a second analog signal; and administering the second analog signal to the second programmable device.

32. The method of claim 26 wherein the first and second DACs are respectively programmed in series with one another.

33. The method of claim 32 wherein the memory administration system includes a routing system and the first and second DACs are respectively programmed using the routing system.

34. The method of claim 33 wherein the routing system includes a demultiplexer circuit and the first and second DACs are respectively programmed using the demultiplexer circuit.

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