HIGH ACCURACY DIRECT READING CAPACITANCE-TO-VOLTAGE CONVERTER

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

This invention relates to a relatively simple and low-cost circuit configuration that implements a capacitance-to-voltage converter which is highly immune to stray capacitance and which accurately measures the unknown capacitance of a capacitor.

2. PRIOR ART

Existing capacitive-type sensors are known which are characterized by considerable stray capacitance-to-ground as a consequence of bonding wires, connectors, headers, ground shields, etc. For example, capacitive-type pressure transducers sense pressure by undergoing a change in dimension, whereby capacitance is a function of applied pressure. The change in capacitance for a full scale pressure change may be only a few picofarads. This small change is difficult to measure in the presence of high stray capacitance-to-ground which may vary with temperature, shock and vibration. More particularly, sophisticated capacitor bridges, RC and LC oscillator-type circuits, and RC charge and discharge time-based circuits are either sensitive to stray capacitance or require highly accurate standard capacitors, such that the cost of the measurement equipment or circuitry may far exceed the cost of the sensor.

Occasionally, it is desirable to measure small capacitors, such as integrated circuit MOS capacitors. Due to the small size of these capacitors, it is difficult to accurately measure the capacitance values thereof while using conventional measurement techniques. Morever, the stray capacitance of the test fixtures also interferes with obtaining a precise measurement of capacitance. On-chip integrated capacitance-to-voltage conversion circuits are available which attempt to reduce the effect of stray capacitance and provide a more accurate measurement of such small capacitors. These conversion circuits use switched capacitor techniques that generate a voltage or digital work which is proportional to capacitance or the difference between a reference capacitor and an unknown capacitor. However, the accuracy of these conversion circuits is degraded by clock feed-through and nonlinearities. Moreover, such circuits are also characterized by limited resolution.

Precise measurement of capacitance is usually accomplished by comparing an unknown value of capacitance with a known value using a bridge circuit. Extremely accurate and high resolution (to 1 ppm) shielded capacitor bridges have been constructed and are used in metrology laboratories. However, a high degree of skill is required to operate these instruments in order to achieve accurate results on small capacitors, since the measurement is greatly influenced by the stray capacitance of conventional test fixtures.

Other capacitance measurement instruments depend upon accurately measuring the charge and discharge times of RC circuits. Such instruments are popular because of their simplicity and compatibility with the single chip digital voltmeter integrated circuit. Unfortunately, such instruments have limited resolution and are very sensitive to stray capacitances of test fixtures or test leads.

Still other techniques indicate capacitance by measuring the impedance of the capacitor using a 4-terminal pair configuration which reduces the effects of stray capacitance. Instruments based upon this technique calculate capacitance from a measurement of reactance. Therefore, such instruments, while being very accurate, are also very complex and expensive.

SUMMARY OF THE INVENTION

Briefly, a circuit is disclosed for implementing a highly accurate, direct reading, capacitance-to-voltage converter which is immune to the effects of stray capacitance-to-ground and by which a measurement is provided of the unknown capacitance of a capacitor. The circuit includes a crystal controlled clock generator which is adapted to supply multi-phase clock signals for controlling the operation of a buffer amplifier and a pair of field effect transistor devices, the conduction paths of which are connected in electrical series between a ground and the current summing junction or virtual ground of a precision operational amplifier. The capacitor under measurement is connected between the output of the buffer amplifier and the series node of the field effect transistor pair.

Operation of the converter circuit is based upon the principle of generating a precise current which is proportional to the unknown capacitance of the capacitor under measurement. The foregoing is accomplished by means of the series connected field effect transistors alternately connecting the capacitor so as to either be charged to a source of reference potential through the buffer amplifier or discharged into the summing junction (or virtual ground) of the precision operational amplifier. More particularly, a pair of non-overlapping clock signals from the clock generator causes the pair of field effect transistors to be alternately rendered conductive, but not conductive at the same time. Accordingly, the field effect transistors successively reverse the leads of the capacitor under measurement between the charge and discharge cycles thereof which tends to reduce errors due to stray capacitance-to-ground. The current which is developed by the periodic discharge of the capacitor under measurement into the summing junction of the operational amplifier generates a voltage at the output of the operational amplifier which is exactly proportional to the capacitance of the capacitor. Thus, by merely reading the voltage at the output terminal of the operational amplifier, an accurate measurement of the capacitance of the capacitor is provided.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a schematic circuit for implementing the highly accurate, direct reading capacitance-to-voltage converter which forms the present invention; and

FIG. **2** is illustrative of the multi-phase clock signals which control the operation of the circuit of FIG. **1**.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The capacitance-to-voltage converter circuit which forms the present invention is now described while referring to the drawings where, in FIG. **1**, there is shown a schematic of the preferred circuit **1**. The timing signals for controlling the operation of the circuit **1** are shown in FIG. **2**. The circuit **1** is implemented by the formation of a crystal controlled oscillator having an amplifier **2** which is connected in a feedback loop to a crystal **4**. The output of the crystal oscillator drives a non-overlapping clock generator **6**. One output terminal of clock generator **6** is connected to an input termi-