semiconductor region with a gate insulating film interposed therebetween;

a source electrode contacting with both the third semiconductor region and the fourth semiconductor region;

a drain electrode for supply of a drain current through the first semiconductor layer;

a fifth semiconductor region of the second conductivity type which is electrically connected to the drain electrode and formed in a given surface region within the second semiconductor layer, so as to pass therethrough a reverse conducting current opposite in direction to the drain current;

a high-voltage withstand region for ensuring a high withstand voltage provided between the fifth semiconductor region and an element region, the element region including at least the third semiconductor region, the fourth semiconductor region and the gate electrode; and

a sixth semiconductor region of the second conductivity type which is formed at or in the vicinity of the interface between the first semiconductor layer and the second semiconductor layer and is provided below at least the element region and the high-voltage withstand region, the sixth semiconductor region having an impurity concentration higher than that of the second semiconductor layer and formed into a given pattern having an extending part extending from the element region to the high-voltage withstand region and windows which are located at least below the element region to allow majority carriers in the first semiconductor layer to pass therethrough, whereby an electric resistance on carriers passing between the fifth semiconductor region and a portion of the second semiconductor layer at a distance from the fifth semiconductor region is reduced but carriers injection between the first semiconductor layer and the second semiconductor layer is allowed.

26. An insulated gate bipolar transistor according to claim **25**, wherein the given pattern of the sixth semiconductor region provides contact portions and non-contact portions between the first and second semiconductor layers, whereby the contact portions allows the carriers injection between the first semiconductor layer and the second semiconductor layer.

27. An insulated gate bipolar transistor according to claim **25**, wherein the sixth semiconductor region is entirely formed in the first semiconductor layer at a close distance from the interface between the first semiconductor layer and the second semiconductor layer, the close distance being smaller than a diffusion length of minority carriers in the first semiconductor layer.

28. An insulated gate bipolar transistor according to claim **25**, wherein the given pattern is a mesh pattern at least below the third semiconductor region.

29. An insulated gate bipolar transistor according to claim **25**, wherein the given pattern is a strip pattern at least below the third semiconductor region.

30. An insulated gate bipolar transistor according to claim **25**, wherein the fifth semiconductor region is formed along a peripheral surface portion of the second semiconductor layer.

31. An insulated gate bipolar transistor according to claim **25**, wherein the sixth semiconductor region is disposed so as to extend from the element region to a region which is below the fifth semiconductor region.

32. An insulated gate bipolar transistor according to claim **31**, wherein the region below the fifth semiconductor region is thoroughly covered with the sixth semiconductor region.

33. An insulated gate bipolar transistor according to claim **31**, wherein the sixth semiconductor region thoroughly covers a region below both the fifth semiconductor region and the high-voltage withstand region.

34. An insulated gate bipolar transistor according to claim **25**, wherein said high-voltage withstand region includes a guard ring.

35. An insulated gate bipolar transistor according to claim **25**, wherein the given pattern is a mesh pattern at least below the element region.

36. An insulated gate bipolar transistor according to claim **25**, wherein the given pattern is a strip pattern at least below the element region.

37. An insulated gate bipolar transistor according to claim **25**, wherein the fifth semiconductor region is formed in a peripheral region which surrounds the element region with the high-voltage withstand region disposed therebetween.

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